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A Novel Single-Stage Common-Ground Transformerless Buck–Boost Inverter

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Abstract: In this article, a novel single-stage transformerless buck–boost inverter is introduced. The proposed inverter can share a common ground between the DC input side and the grid; this leads to having a zero-leakage current. The proposed inverter also provides the buck and boost voltage capabilities. Additionally, the power switches are operated at high frequency in the half-cycle of the sinusoidal wave, so the efficiency of the proposed inverter can be improved. Operating analysis, design consideration, comparison, and simulation study are presented. Finally, a 500 W laboratory prototype is also built to confirm the correctness and feasibility of the proposed inverter.

Keywords: transformerless topology; common ground; buck-boost ability; single-phase single-stage; PV inverter

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1. Introduction

In recent years, the nearly exhausted fossil fuels and environmental deterioration have promoted the development of renewable energy sources such as wind power, photovoltaic (PV), fuel cells, and ocean waves [1–4]. Among these renewable energy sources, the PV market has several advantages, which include being inexhaustible, as well as its easy availability and pollution-free operation. Moreover, the main technological evolution for the PV system is the inverter. The inverter can be divided into two types with transformer topologies [5–7] or transformerless topologies [8–10]. Although transformer-based inverters can provide galvanic isolation and protection, they have undesirable properties such as high cost and weight, with additional losses [9,10]. On the other hand, transformerless inverters have reduced costs and sizes, and improved efficiency, but the isolation between the PV panel and the inverter system leads to the occurrence of leakage current. This leakage current causes a rise in harmonic distortion, in both output voltage and current, which also results in electromagnetic interference between the PV system and grid. To eliminate leakage current, the DC current injection from the inverter should also be reduced, as presented in the standards IEEE 1547 and IEC 61727 [11,12]. Moreover, the transformerless inverter topologies can be classified into two groups—namely, two-stage configurations and single-stage configurations. In two-stage configurations, the power processing is divided into two stages. A DC–DC boost converter is added between the inverter side and DC input power supply side, which boosts a low-voltage input to the high voltage required for the second stage [13–15]. The next stage is an inverter that converts DC voltage to AC voltage to connect with the grid. Two-stage transformerless inverter topologies can have some disadvantages, including low efficiency, increased cost, and complexity control in a two-stage configuration. In contrast, single-stage configurations have all the functions of

boosting ability and maximum power extraction, as well as DC–AC conversion. Compared with two-stage configurations, single-stage configurations have more benefits, including compactness, lower device count, lower costs, and greater efficiency [16]. From this point of view, single-stage inverters are reported in the literature, and their comprehensive review is given in [17–27]. Common-ground transformerless inverter topologies were introduced in [21–25,28–30], which directly connect the ground of the grid to the negative of the DC input source. The common-mode voltage is equal to zero, and it also protects against any high-frequency content. Therefore, there is no common-mode leakage current in the presented topologies.

In order to improve the boosting capability and provide common ground with single-stage configuration, single-stage, common-ground transformerless inverters have been used in [23] without a continuous input current. However, the power switches are operated at high frequency. This leads to an increase in the switching loss of the inverter. Similarly, a buck–boost inverter in [24] with five switches is proposed to achieve the common-ground condition and wide buck–boost voltage operation. However, three switches are operated at a high switching frequency in the half-line period. The single-phase transformerless grid-connected PV inverter introduced in [25,26] also focuses on a doubly grounded inverter with single-stage conversion and uses fewer components. Nevertheless, the disadvantage of this inverter is also the high switching frequency of its power switches. To further improve the voltage gain, a novel step-up transformerless inverter is presented in [27]. This inverter can provide the common ground between the output and input sides with a single stage. However, it requires more switches, which increases the size and cost of the inverter package.

In this article, a novel single-stage common-ground transformerless buck–boost inverter (CGBBI) is proposed to eliminate leakage current elimination and achieve voltage boosting capability. Moreover, the PWM control method of the proposed inverter can reduce the high switching loss on semiconductor devices. The remainder of this article is organized as follows: First, the inverter configuration, PWM control method, and operating principle of the proposed inverter are presented in Section 2. Design guidelines of the devices are given in Section 3. A comparative study is provided in Section 4, drawing on other existing common-ground buck–boost inverter topologies. Simulation and experimental results are presented in Section 5 to evaluate the accurate performance of the proposed inverter. Finally, the conclusions of the study are drawn in Section 6.

2. Derivation of Proposed CGBBI

The proposed CGBBI topology is shown in Figure 1. The major characteristic of the proposed CGBBI topology is to have a common point between the output side and the negative terminal of the input DC power supply, which avoids the leakage current [9]. The proposed CGBBI topology includes five power switches S_1–S_5, three diodes D_1–D_3, two inductors L_1–L_2, two capacitors C_1–C_2, and one output filter inductor L_f. It can be seen that the proposed CGBBI topology is composed of one buck–boost module, one boost module, and one power switch operating at low frequency. The buck–boost module comprises three power switches S_1–S_3, two diodes D_1–D_2, and a pair of L_1 and C_1. Similarly, the boost module has one power switch S_4, one diode D_3, one inductor L_2, and one capacitor C_2.

2.1. PWM Control Method for the Proposed CGBBI Topology

Figure 2 presents the PWM control method for the proposed CGBBI topology. When output voltage v_o is higher than 0, switch S_3 is turned on, and S_4 and S_5 are turned off. However, switches S_1 and S_2 are turned on/off alternately at high frequency. When the output voltage v_o is negative, three switches S_1, S_2, and S_3 are turned off, while S_5 is turned on. In this case, only switch S_4 is operated at high frequency during this negative half-line cycle.

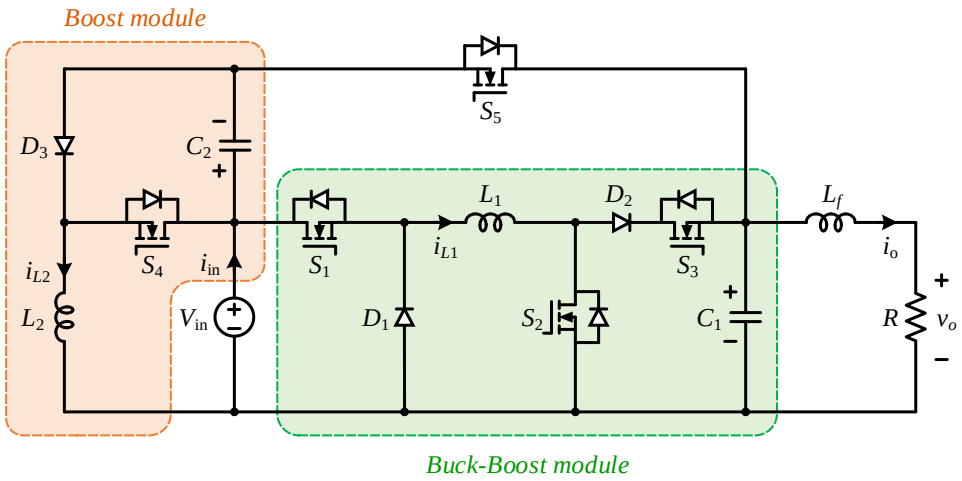

Figure 1. Proposed single-stage common-ground buck–boost inverter.

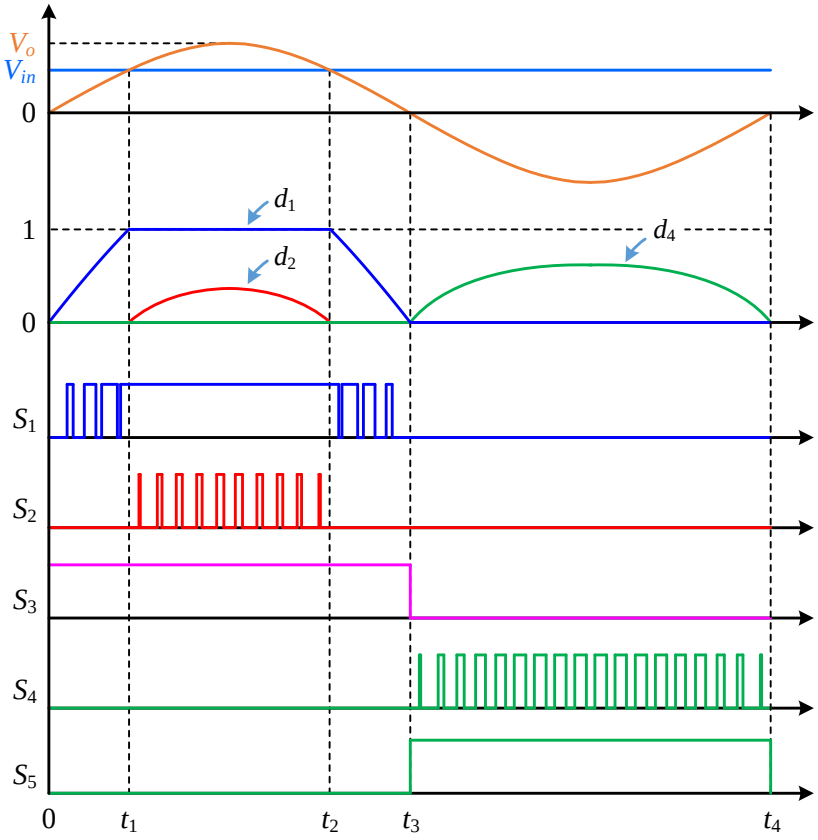

Figure 2. PWM control method of the proposed CGBBI topology.

2.2. Operating of the Proposed CGBBI Topology

Interval 1 ([0, t_1] or [t_2, t_3]): This interval appears when the voltage V_{in} is higher than v_o. In this case, only the buck–boost module is operated. Switch S_3 is turned on, while S_2, S_4, and S_5 are turned off. It can be seen that only switch S_1 is turned on and off at high frequency. Voltage v_{C1} is equal to v_o. In terms of the inductor current, i_{L1} approximates the output current, while i_{L2} is zero.

Mode 1 (Figure 3a): Switch S_1 is turned off, and diodes D_1–D_2 are forward biased. Inductor L_1 is connected to the capacitor C_1 and load, to which it charges energy. In this

mode, capacitor C_1 provides energy to the load and maintains the constant output voltage across the load. We have

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = -v_o \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_o \end{cases} \quad (1)$$

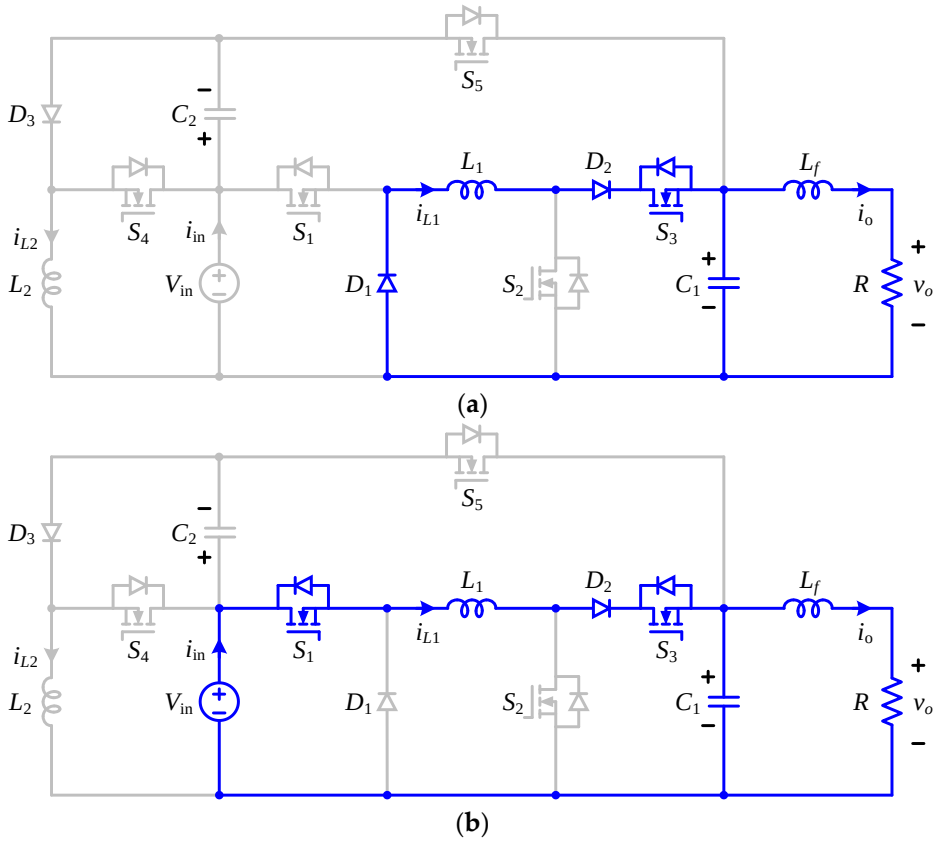

Figure 3. Equivalent circuits of the proposed CGBBI topology in interval 1 when $0 < v_o < V_{in}$: (**a**) mode 1 and (**b**) mode 2.

Mode 2 (Figure 3b): Switch S_1 is turned on, diode D_1 is reverse biased and D_2 is forward biased. Inductor L_1 is charged by an input voltage V_{in}, capacitor C_1, and the load. The inductor current i_{L1} increases linearly. The equations in this mode can be derived as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - v_o \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_o \end{cases} \quad (2)$$

By applying voltage-second balance condition to an inductor L_1, the relationship between v_o and V_{in} can be obtained as

$$v_o = d_1 V_{in} \quad (3)$$

where d_1 is the duty ratio of S_1.

Interval 2 ($[t_1, t_2]$): This interval appears when the input voltage V_{in} is lower than v_o. In this case, only the buck–boost module operates. Switch S_1 is turned on, while S_4 and S_5 are kept off. Only switch S_2 is turned on and off at high frequency. Voltage v_{C1} is equal to v_o, while inductor current i_{L1} is larger than output current, and inductor current i_{L2} is zero.

Mode 1 (Figure 4a): Switch S_2 in the buck–boost converter is turned on. Consequently, diodes D_1 and D_2 are reverse biasED. The voltage in inductor L_1 equals the input voltage

V_{in}. Inductor current i_{L1} increases linearly, and capacitor C_1 charges the load. The related equations are as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} \\ C_1 \frac{dv_{C1}}{dt} = -i_o \end{cases} \tag{4}$$

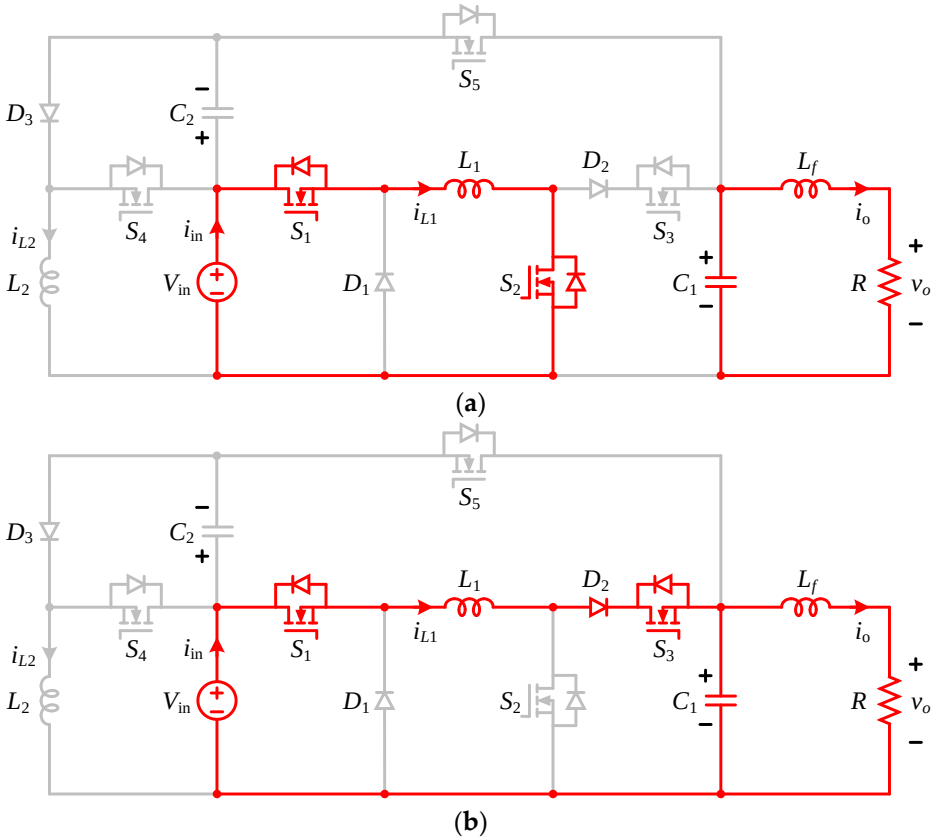

Figure 4. Equivalent circuits of the proposed CGBBI topology in interval 2 when $v_o > V_{in}$: (**a**) mode 1 and (**b**) mode 2.

Mode 2 (Figure 4b): Switch S_2 is turned off, diode D_1 is reverse biased, and D_2 is forward biased. The power supply and inductor L_1 charge energy to filter the capacitor and the load, so capacitor C_1 is charged, and inductor current i_{L1} decreases linearly. We have

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - v_o \\ C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_o \end{cases} \tag{5}$$

The relationship between v_o and V_{in} can be obtained from (4) and (5).

$$v_o = \frac{V_{in}}{1 - d_2} \tag{6}$$

where d_2 is the duty ratio of S_2.

Interval 3 ($[t_3, t_4]$): The output voltage is negative, and it can be observed that only the boost module operates in this interval. Switch S_5 is turned on and switches S_1, S_2, and S_3 are turned off. In this case, only switch S_4 is controlled at high frequency. Voltage v_{C1} is equal to output voltage v_o. Capacitor voltage v_{C2} is the total voltage of input voltage and output voltage, while inductor current i_{L1} is equal to 0, and inductor current i_{L2} is higher than the output current.

Mode 1 (Figure 5a): Switch S_4 is turned on, and diode D_3 is reverse biased in this mode. Inductor L_2 is charged from the input voltage, and the inductor current i_{L2} increases

linearly. The capacitor C_2 transfers power to the load. The equations of this mode can be found as follows:

$$\begin{cases} L_2 \frac{di_{L2}}{dt} = V_{in} \\ C_2 \frac{dv_{C2}}{dt} = i_{in} - i_{L2} \\ C_1 \frac{dv_{C1}}{dt} = i_{in} - i_{L2} - i_o \end{cases} \tag{7}$$

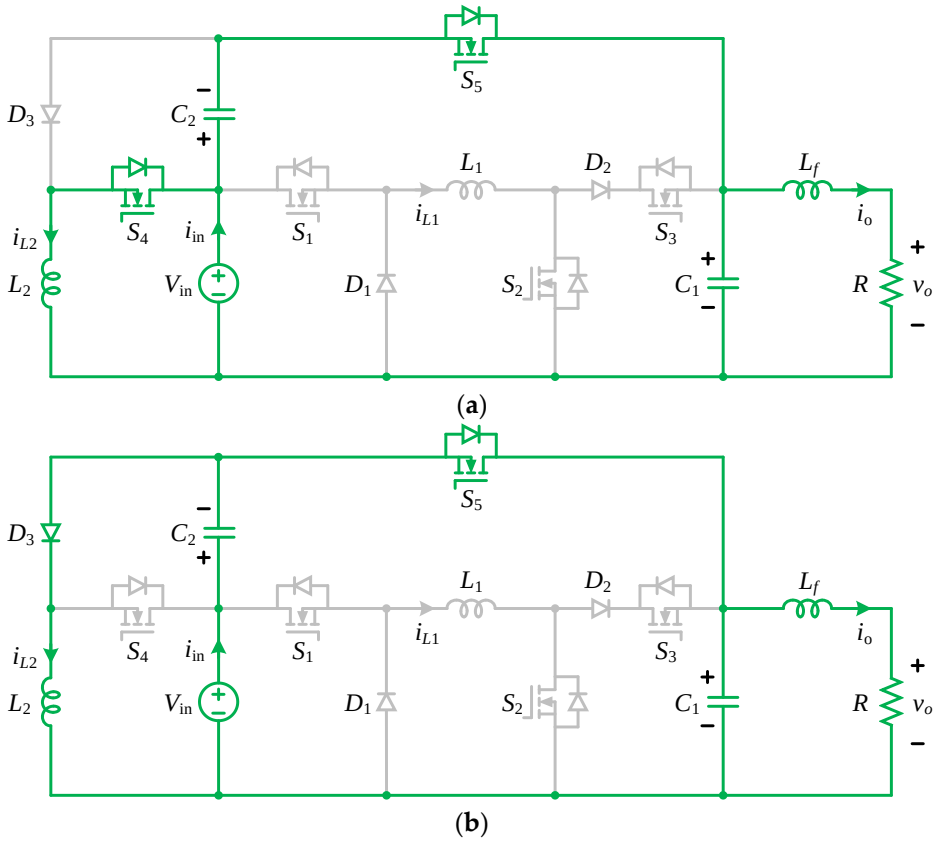

Figure 5. Equivalent circuits of the proposed CGBBI topology in interval 3 when $v_o < 0$: (**a**) mode 1 and (**b**) mode 2.

Mode 2 (Figure 5b): Switch S_4 is turned off, and diode D_3 is forward biased. Inductor L_2 transfers energy to capacitor C_2 through diode D_3. In this mode, the energy of inductor L_2 is also transferred to capacitor C_1 and the load through S_5 and D_3, so the inductor current i_{L2} decreases linearly. We have

$$\begin{cases} L_2 \frac{di_{L2}}{dt} = V_{in} - v_{C2} \\ C_2 \frac{dv_{C2}}{dt} = i_{in} \\ C_1 \frac{dv_{C1}}{dt} = i_{in} - i_o - i_{L2} \end{cases} \tag{8}$$

From (7) and (8), we have

$$v_o = \frac{d_4 V_{in}}{d_4 - 1} \tag{9}$$

where d_4 is the duty ratio of S_4.

When $v_o > 0$, the voltage in capacitors C_1 and C_2 can be given as

$$\begin{cases} v_{C1} = V_o sin\omega t \\ v_{C2} = V_{in} \end{cases} \tag{10}$$

When $v_o < 0$, the voltage in capacitors C_1 and C_2 can be rewritten as

$$\begin{cases} v_{C1} = V_o sin\omega t \\ v_{C2} = V_{in} - V_o sin\omega t \end{cases} \tag{11}$$

where V_o is the peak value of output voltage, and ω is the angular frequency.

The relationship between the input voltage and the peak value of output voltage can be determined as follows:

$$M = \frac{V_o}{V_{in}} \tag{12}$$

where M is the modulation index.

The resulting duty cycles for the PWM modulation are visualized in Figure 2 and are calculated based on (12).

From (3), (6), (9), (12), the corresponding duty cycles for the PWM control method are defined in (13) and (14) as follows:

$$\begin{cases} d_1(t) = Msin\omega t \\ d_2(t) = 1 - \frac{1}{Msin\omega t} \\ d_4(t) = 0 \end{cases}, when\ v_o > 0 \tag{13}$$

$$\begin{cases} d_1(t) = 0 \\ d_2(t) = 0 \\ d_4(t) = \frac{Msin\omega t}{Msin\omega t - 1} \end{cases}, when\ v_o < 0 \tag{14}$$

According to (13) and (14), the maximum values of the corresponding duty cycles can be expressed as

$$\begin{cases} D_{1.max} = M \\ D_{2.max} = 1 - \frac{1}{M}\ with\ M > 1 \\ D_{2.max} = 0\ with\ M \leq 1 \\ D_{4.max} = \frac{M}{M+1} \end{cases} \tag{15}$$

In order to determine the switching state in the PWM control method, shown in Figure 2, interval 2 is executed when the output voltage is higher than the input voltage. The values of t_1 and t_2 are calculated as follows:

$$\begin{cases} t_1 = \frac{1}{\omega} sin^{-1}\left(\frac{1}{M}\right) \\ t_2 = \pi - \frac{1}{\omega} sin^{-1}\left(\frac{1}{M}\right) \end{cases} \tag{16}$$

3. Parameter Design

3.1. Selection of the Inductors

Using (1), (2), (4), (5), (7), and (8), applying the volt-second balance principle on L_1 and L_2, the inductors L_1 and L_2 currents can be calculated using (17) and (18).

$$i_{L1} = \begin{cases} I_o sin\omega t,\ 0 < t \leq t_1\ and\ t_2 < t \leq t_3 \\ \frac{I_o sin\omega t}{1 - d_2},\ t_1 < t \leq t_2 \\ 0,\ t_3 < t \leq t_4 \end{cases} \tag{17}$$

$$i_{L2} = \begin{cases} 0,\ 0 < t \leq t_3 \\ \frac{I_o sin\omega t}{d_4 - 1},\ t_3 < t \leq t_4 \end{cases} \tag{18}$$

where I_o is the peak value of output current.

According to (17), (18), and (12), the peak value of inductors L_1 and L_2 currents can be given by (19) and (20).

$$I_{L1} = \begin{cases} I_o,\ M \leq 1 \\ MI_o,\ M > 1 \end{cases} \tag{19}$$

$$I_{L2} = (M+1)I_o \tag{20}$$

The inductors can be designed by using the equation of their current ripple, using (17), (18), and (15), while the peak-to-peak current ripple of inductors L_1 and L_2 can be defined by (21) and (22).

$$\Delta i_{L1.max} = \begin{cases} \frac{V_{in}}{4f_s L_1}, & M \leq 1 \\ \frac{(M-1)V_{in}}{Mf_s L_1}, & M > 1 \end{cases} \tag{21}$$

$$\Delta i_{L2.max} = \frac{MV_{in}}{(M+1)f_s L_2} \tag{22}$$

where f_s denotes the switching frequency.

According to (19)–(22), the inductance values of L_1 and L_2 can be calculated using (23) and (24) as follows:

$$L_1 = \begin{cases} \frac{V_{in}}{4f_s x\% I_o}, & M \leq 1 \\ \frac{(M-1)V_{in}}{M^2 f_s x\% I_o}, & M > 1 \end{cases} \tag{23}$$

$$L_2 = \frac{MV_{in}}{(M+1)^2 f_s x\% I_o} \tag{24}$$

where $x\%$ is the inductors L_1 and L_2 ripple.

Based on the maximum value of the current through the inductors L_1, L_2 in (19) and (20). The stored energy of the inductor is given by

$$W_m = \frac{1}{2} L I_{L.max}^2 \tag{25}$$

The required area product of the inductor, as cited in [31,32], is

$$A_p = \frac{2W_m}{K_u B_m J_m} \tag{26}$$

where K_u, B_m, and J_m are the core window of the fill factor, the amplitude of a magnetic flux density in the core, and the amplitude in current density of the winding conductor, respectively.

3.2. Selection of the Capacitors

Using the equations given in (15), the peak-to-peak voltage ripple of capacitors C_1 and C_2 can be defined as

$$\Delta v_{C1.max} = \begin{cases} \frac{V_{in}}{32L_1 C_1 f_s^2}, & M \leq 1 \\ \frac{(M-1)I_o}{Mf_s C_1}, & M > 1 \end{cases} \tag{27}$$

$$\Delta v_{C2.max} = \frac{MI_o}{(M+1)f_s(C_1 + C_2)} \tag{28}$$

According to (27) and (28), the capacitance values of C_1 and C_2 are calculated as follows:

$$C_1 = \begin{cases} \frac{V_{in}}{32yL_1 f_s^2}, & M \leq 1 \\ \frac{(M-1)I_o}{Mf_s y\% V_o}, & M > 1 \end{cases} \tag{29}$$

$$C_2 = \frac{MI_o}{(M+1)f_s y\% V_o} - C_1 \tag{30}$$

where $y\%$ is the capacitors C_1 and C_2 ripple.

3.3. Selection of Switching Devices

The voltage stress across the switches and the diodes are given in (31)–(34).

$$\begin{cases} V_{DS1} = V_{D1} = V_{in} \\ V_{DS2} = V_{DS3} = V_{DS5} = V_{D2} = V_o \\ V_{DS4} = V_{D3} = V_{in} + V_o \end{cases} \tag{31}$$

The current stresses of switches S_1–S_5 reach the maximum when the output current has its peak value (I_o), as given by (32)–(34).

$$\begin{cases} I_{S1} = I_{S3} = I_{D1} = I_{D2} = I_{L1} = I_o \\ I_{S2} = 0 \end{cases}, \; M \leq 1 \tag{32}$$

$$\begin{cases} I_{S1} = I_{S2} = I_{S3} = I_{D2} = I_{L1} = MI_o \\ I_{D1} = I_o sin\omega t_1 \end{cases}, \; M > 1 \tag{33}$$

$$I_{S5} \approx I_{S4} = I_{D3} = I_{L2} = (M+1)I_o \tag{34}$$

3.4. Power Loss Calculation

3.4.1. Power Loss of Power Switches

The total power loss of the switches is equal to the sum of the conduction losses and switching losses, given by

$$P_{S\_tot} = P_{S\_con} + P_{S\_sw} \tag{35}$$

$$P_{S\_con} = \sum_{i=1}^{5} R_{dsi} I_{Si.rms}^2 \tag{36}$$

$$P_{S\_sw} = \sum_{i=1}^{5} V_{Si} I_{Si.avg} \left(t_{ri} + t_{fi} \right) f_s \tag{37}$$

where R_{dsi}, t_{ri}, and t_{fi} are the on-state drain-source resistance, the turn-on and turn-off delay times of each MOSFET, respectively.

The average and RMS current values through the switches are calculated as

$$\begin{cases} I_{S1.avg} = \frac{1}{2\pi}\left[2\int_0^{t_1} i_{L1}(t) d_1(t) d(\omega t) + \int_{t_1}^{t_2} i_{L1}(t) d(\omega t)\right] \\ I_{S1.rms} = \sqrt{\frac{1}{2\pi}\left[2\int_0^{t_1} {i_{L1}}^2(t) d_1(t) d(\omega t) + \int_{t_1}^{t_2} {i_{L1}}^2(t) d(\omega t)\right]} \end{cases} \tag{38}$$

$$\begin{cases} I_{S2.avg} = \frac{1}{2\pi}\left[\int_{t_1}^{t_2} i_{L1}(t) d_2(t) d(\omega t)\right] \\ I_{S2.rms} = \sqrt{\frac{1}{2\pi}\left[\int_{t_1}^{t_2} {i_{L1}}^2(t) d_2(t) d(\omega t)\right]} \end{cases} \tag{39}$$

$$\begin{cases} I_{S3.avg} = \frac{1}{2\pi}\left[\int_{t_1}^{t_2} i_{L1}(t)[1 - d_2(t)] d(\omega t)\right] \\ I_{S3.rms} = \sqrt{\frac{1}{2\pi}\left[\int_{t_1}^{t_2} {i_{L1}}^2(t)[1 - d_2(t)] d(\omega t)\right]} \end{cases} \tag{40}$$

$$\begin{cases} I_{S4.avg} = \frac{1}{2\pi}\left[\int_{\pi}^{2\pi} i_{L2}(t) d_4(t) d(\omega t)\right] \\ I_{S4.rms} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi}^{2\pi} {i_{L2}}^2(t) d_4(t) d(\omega t)\right]} \end{cases} \tag{41}$$

$$\begin{cases} I_{S5.avg} = \frac{1}{2\pi}\left[\int_{\pi}^{2\pi} [i_{L2}(t) - I_{in}][1 - d_4(t)] d(\omega t)\right] \\ I_{S5.rms} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi}^{2\pi} [i_{L2}(t) - I_{in}]^2[1 - d_4(t)] d(\omega t)\right]} \end{cases} \tag{42}$$

3.4.2. Power Loss of Diodes

The power loss in the diodes includes conduction loss and reverse recovery loss. The power loss of the diodes is calculated as

$$P_{D\_tot} = P_{D\_con} + P_{D\_sw} \tag{43}$$

$$P_{D\_con} = \sum_{i=1}^{3} \left(V_{Fi} I_{Di.avg} + R_{Di} I_{Di.rms}^2 \right) \tag{44}$$

$$P_{D\_sw} = \sum_{i=1}^{3} Q_{rri} V_{Di} f_s \tag{45}$$

where V_{Fi}, R_{Di}, and Q_{rri} are the forward voltage, the ON-state resistance, and the reverse recovery charge of each diode, respectively.

The average and RMS current values through the switches are calculated as

$$\begin{cases} I_{D1.avg} = \frac{1}{\pi} \int_0^{t_1} i_{L1}(t)[1 - d_1(t)] d(\omega t) \\ I_{D1.rms} = \sqrt{\frac{1}{\pi} \int_0^{t_1} {i_{L1}}^2(t)[1 - d_1(t)] d(\omega t)} \end{cases} \tag{46}$$

$$\begin{cases} I_{D2.avg} = \frac{1}{2\pi} \int_{t_1}^{t_2} i_{L1}(t)[1 - d_2(t)] d(\omega t) \\ I_{D2.rms} = \sqrt{\frac{1}{2\pi} \int_{t_1}^{t_2} {i_{L1}}^2(t)[1 - d_2(t)] d(\omega t)} \end{cases} \tag{47}$$

$$\begin{cases} I_{D3.avg} = \frac{1}{2\pi} \int_{\pi}^{2\pi} i_{L2}(t)[1 - d_4(t)] d(\omega t) \\ I_{D3.rms} = \sqrt{\frac{1}{2\pi} \int_{\pi}^{2\pi} {i_{L2}}^2(t)[1 - d_4(t)] d(\omega t)} \end{cases} \tag{48}$$

3.4.3. Power Loss of Inductors

The power loss in the inductors includes the core loss and copper loss. The inductor loss is defined as

$$P_L = 2 \cdot k \cdot B^{\beta} \cdot f_s^{\alpha} \cdot A_e \cdot l_e + r_L \left(I_{L1.rms}^2 + I_{L2.rms}^2 \right) \tag{49}$$

where B is the AC magnetic flux; f_s is the frequency; A_e is the core cross-sectional area; l_e is the core mean magnetic path length; $I_{L1.rms}$ and $I_{L2.rms}$ are RMS currents of the inductors; r_L is wire resistance. k, α, and β can be found in the manufacturer's datasheet.

RMS values $I_{L1.rms}$ and $I_{L2.rms}$ can be calculated as

$$\begin{cases} I_{L1.rms} = \sqrt{\frac{1}{2\pi} \left(2 \int_0^{t_1} {i_o}^2(t) d(\omega t) + \int_{t_1}^{t_2} \left[\frac{i_o(t)}{1 - d_2(t)} \right]^2 d(\omega t) \right)} \\ I_{L2.rms} = \sqrt{\frac{1}{2\pi} \int_{\pi}^{2\pi} \left[\frac{i_o(t)}{1 - d_4(t)} \right]^2 d(\omega t)} \end{cases} \tag{50}$$

3.4.4. Power Loss of Capacitors

The power loss of capacitors is calculated as

$$P_C = r_{C1} I_{C1.rms}^2 + r_{C2} I_{C2.rms}^2 \tag{51}$$

where r_{C1} and r_{C2} are the equivalent series resistance (ESR) of the C_1 and C_2 capacitors, respectively; $I_{C1.rms}$ and $I_{C2.rms}$ are the RMS capacitor currents and are calculated as

$$\begin{cases} I_{C1.rms} = \sqrt{\frac{1}{2\pi} \left(\int_{t_1}^{t_2} {i_o}^2(t) d_2(t) d(\omega t) + \int_{\pi}^{2\pi} [I_{in} - i_{L2}(t) - i_o(t)]^2 d(\omega t) \right)} \\ I_{C2.rms} = \sqrt{\frac{1}{2\pi} \left(\int_{\pi}^{2\pi} [I_{in} - i_{L2}(t)]^2 d_4(t) d(\omega t) + \int_{\pi}^{2\pi} {I_{in}}^2 [1 - d_4(t)] d(\omega t) \right)} \end{cases} \tag{52}$$

4. Comparison with Other Common-Ground Transformerless Inverters

Currently, the research literature is often focused on extending the buck–boost ability with higher efficiency, reducing the number of devices, and decreasing voltage stress across semiconductor devices. To show the potential capability of the proposed CGBBI topology, a comparative analysis between the proposed CGBBI topology and other common-ground transformerless inverters is presented in Table 1. It can be seen that the number of devices in the inverters proposed by [21,23] is lower than that of the inverters developed by [22,24,25], as well as the proposed CGBBI of this study. Moreover, the total number of devices in the proposed CGBBI is lower than that of the inverter in [22,24]. Having considered voltage stress across the power switches, the inverter developed by [22] and our proposed CGBBI have total switch voltage stress of $2V_{in} + 4V_o$, which is lower than that of the inverter in [21,23–25]. As is clear from Table 1, the number of high-frequency switches in each period in the proposed CGBBI topology is the least when compared with other inverters. When comparing diode voltage stress values, it is revealed that the inverter used in [25] and the proposed CGBBI have lower voltage stress values than the inverters in [22,24]. Compared with the inverters in [28,29], the proposed CGBBI requires a smaller number of power switches than that in [28,29] and the number of high-frequency switches in each period in the inverters developed by [28,29] is higher than that of the proposed CGBBI. In addition, the number of devices in the inverter used in [30] is equal to that of the proposed CGBBI. However, the total voltage stress of semiconductor devices in the proposed CGBBI is smaller than that in the inverter [30]. Considering the comparison in terms of component count, the voltage stress on semiconductor devices, and the number of high-frequency switches, the proposed CGBBI topology is a better solution than other common-ground buck–boost inverters mentioned in the literature.

Table 1. Comparison between the proposed CGBBI topology and other common-ground transformerless inverters.

	Inverter in [21]	Inverter in [22]	Inverter in [23]	Inverter in [24]	Inverter in [25]	Inverter in [28]	Inverter in [29]	Inverter in [30]	Proposed CGBBI
Switches	4	6	5	5	5	8	7	5	5
Diodes	2	5	0	4	3	0	1	3	3
Inductors	2	2	2	5	2	1	0	2	2
Capacitors	2	1	2	3	2	1	2	2	2
Total devices	10	14	9	17	12	10	10	12	12
Switches stress	S_1 to S_4: $2V_o$	S_1, S_4: V_{in} S_2, S_3: V_o S_5, S_6: V_o	S_1 to S_5: $V_{in} + V_o$	S_1 to S_5: $V_{in} + V_o$	S_1: $V_{in} + V_o$ S_2 to S_5: V_o	S_1: V_{in} S_2: V_o S_3: V_{in} S_4, S_7: $V_{in} + V_o$ S_5: V_o S_6, S_8: V_o	S_1, S_2: V_{in} S_3: $3V_{in}$ S_4, S_5: $2V_{in}$ S_6: $2V_{in}$ S_7: $4V_{in}$	S_1, S_2: $V_{in} + V_o$ S_3, S_4: V_o S_5: V_o	S_1: V_{in} S_2, S_3, S_5: V_o S_4: $V_{in} + V_o$
HF-switches in each period	$4P$ $4N$	$3P$ $3N$	$2P$ $2N$	$3P$ $1N$	$3P$ $1N$	$5P$ $3N$	$4P$ $5N$	$2P$ $1N$	$2P$ $1N$
Diodes stress	-	D_1, D_4: V_{in} D_2, D_3, D_5: V_o	-	D_1 to D_4: $V_{in} + V_o$	D_1: $V_{in} + V_o$ D_2: V_{in} D_3: V_o	-	D: V_{in}	D_1: V_o D_2: $V_{in} + V_o$ D_3: $V_o - V_{in}$	D_1: V_{in} D_2: V_o D_3: $V_{in} + V_o$

P and N are the number of high-frequency switching in positive and negative half-line periods, respectively.

5. Simulation and Experiment Verifications

5.1. Simulation Results

The operating analysis of the proposed CGBBI topology was verified in the PSIM simulation version 9.1 [33]. The specifications for simulation are shown in Table 2. The drain-to-source on-resistance and body-diode threshold voltage of the MOSFETs S_1, S_4, and S_2, S_3, S_5 were set to 25.5 mΩ, 45 mΩ, and 8 mΩ, respectively. The forward voltage of diodes D_1 to D_3 was set to 1.12 V, 0.7 V, and 1.4 V, respectively. Figures 6 and 7 present the simulation waveforms of the proposed CGBBI topology in both buck and boost operations. The RMS values of the output voltage and output frequency were set at 110 V and 50 Hz.

The input voltage values were 60 V and 240 V. In the case of V_{in} = 60 V, the modulation index and maximum values of duty cycles were M = 2.58, $D_{1.\max}$ = 2.58, $D_{2.\max}$ = 0.61, $D_{4.\max}$ = 0.72. Additionally, with V_{in} = 240 V, the modulation index and maximum values of duty cycles were M = 0.64, $D_{1.\max}$ = 0.64, $D_{2.\max}$ = 0, $D_{4.\max}$ = 0.39. The high-switching frequency of semiconductor devices was 50 kHz. From the design guideline in Section 3, the parameters of passive devices were chosen as follows: L_1 = L_2 = 0.5 mH, C_1 = 5 µF, C_2 = 1 µF. The input voltage, capacitor C_2 voltage, output voltage, voltage stresses of semiconductor devices are shown in Figures 6 and 7. Moreover, the THD values of the output voltage waveforms were measured at 1.2% and 0.5% for the input voltage of 60 V and 240 V, respectively. It can be observed that the simulation results well agreed with the theoretical analysis. The conduction and switching losses of the proposed CGBBI, together with the simulation results, are shown in Table 3. It can be seen that the simulation results are close to the power loss analysis.

Table 2. Parameters of the proposed CGBBI topology.

Parameter	Symbol	Part No./Value
Input voltage range	V_{in}	60–240 V
Output Voltage	v_o	110 Vrms
Output frequency	f_o	50 Hz
Output Power	P_o	500 W
Switching frequency	f_{sw}	50 kHz
Capacitors	C_1	5 µF/200 V
	C_2	1 µF/450 V
Inductors	L_1, L_2	0.5 mH
Filter inductor	L_f	0.5 mH
MOSFETs	S_1	IRFP4868PbF (300 V, 70 A, R_{dson} = 25.5 mΩ)
	S_2, S_3, S_5	IRFP4668PbF (200 V, 130 A, R_{dson} = 8 mΩ)
	S_4	IPW60R045CPA (600 V, 60 A, R_{dson} = 45 mΩ)
Diodes	D_1	FF60UP30DN (300 V, 60 A, V_F = 1.12 V)
	D_2	STPS60SM200C (200 V, 30 A, V_F = 0.7 V)
	D_3	DSEI30-06A (600 V, 37 A, V_F = 1.4 V)

Table 3. The power loss of the proposed CGBBI with simulation.

Components	V_{in} = 60 V				V_{in} = 240 V			
	Currents (A)		Losses (W)		Currents (A)		Losses (W)	
	Average	RMS	Conduction	Switching	Average	RMS	Conduction	Switching
S_1	4.1	7.08	1.28	0.75	1.04	2.4	0.15	1.25
S_2	2.14	5.33	0.23	2.97	0	0	0	0
S_3	2	4.67	0.17	2.77	2.05	3.26	0.09	2.84
S_4	4.12	8.53	3.27	1.33	1.03	2.99	0.4	1.63
S_5	2	4.54	0.16	2.77	2.05	3.65	0.11	2.84
D_1	5.24×10^{-2}	0.26	0.06	0.03	1.01	2.19	1.28	0.13
D_2	2	4.67	1.9	0	2.05	3.26	1.68	0
D_3	2	5.62	4.38	0.94	2.06	4.05	3.7	1.73
L_1	4.15	7.09	2.01	-	2.05	3.25	0.42	-
L_2	6.12	10.22	4.18	-	3.09	5.04	1.02	-
C_1	1.9×10^{-3}	4.77	0.11	-	3.86×10^{-3}	1.77	0.02	-
C_2	9.22×10^{-3}	1.48	0	-	9.32×10^{-3}	0.77	0	-
P_{loss}	-	-	29.31		-	-	19.29	

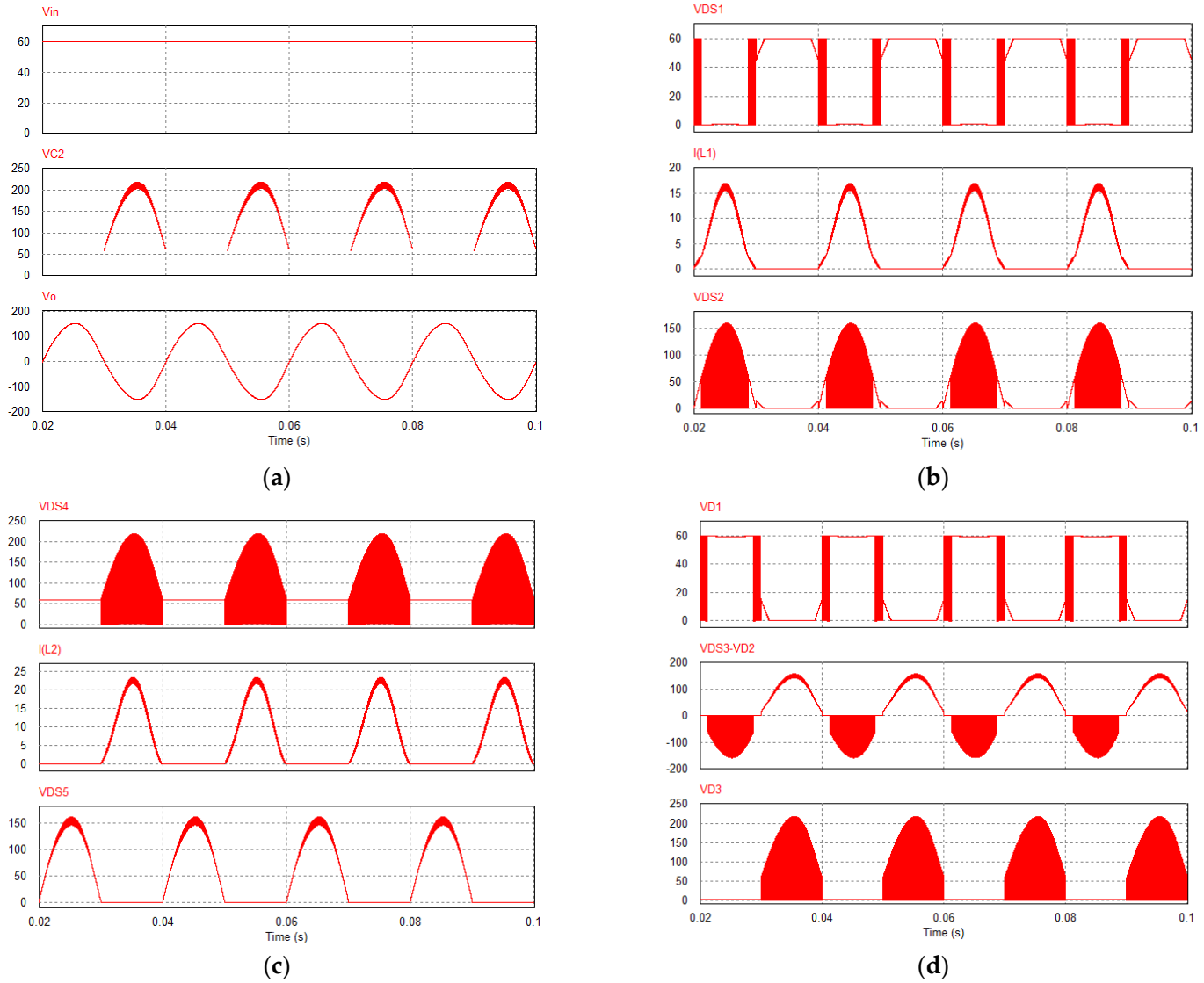

Figure 6. Simulation results with V_{in} = 60 V: (**a**) the input, output and capacitor C_2 voltages, (**b**) the voltage stress on switches S_1, S_2, and the current of inductor L_1, (**c**) the voltage stress on switches S_4, S_5, and the current of inductor L_2, and (**d**) the voltage stress on diodes D_1, D_2, D_3 and the voltage stress on switch S_3.

5.2. Experimental Results

A 500 W prototype circuit was fabricated and tested to verify the performance of the proposed CGBBI topology. The specifications for testing are also shown in Table 2. Figure 8 presents the experimental waveforms of the proposed CGBBI topology when the inverter operated in boost mode. The maximum value of the output voltage was boosted to 155 V from an input voltage of 60 V, which corresponds to M = 2.58. Figure 8a shows the input voltage, capacitor C_2 voltage, and output voltage for the load value of 24 Ω and filter inductor of 0.5 mH. The capacitor voltage V_{C2} was half-sinusoidal with DC offset V_{in} in the positive half of the output cycle. Therefore, the peak voltage across the capacitor C_2 was approximately 220 V. In the negative half of the output cycle, the voltage across the capacitor C_1 was equal to the input voltage. The RMS value and THD of the output voltage waveform were 109 V and 1.6%, respectively. Figure 8b shows the voltage stress on switches S_1, S_2, and the current of inductor L_1. Figure 8c shows the voltage stress on switches S_4, S_5, and the current of inductor L_2. The peak currents of inductors L_1 and L_2 were about 16 A and 23 A, respectively. The high-frequency ripple of inductors L_1 and L_2

current were about 2.5 A and 3 A, respectively. Figure 8d shows the voltage stress on diode D_1, the voltage stress on switch diodes S_3–D_2, and voltage stress on diode D_3. Similarly, the proposed CGBBI topology was tested with an input voltage of 240 V, as shown in Figure 9. It can be seen that the experimental results are verified with the simulation and the theoretical analyses.

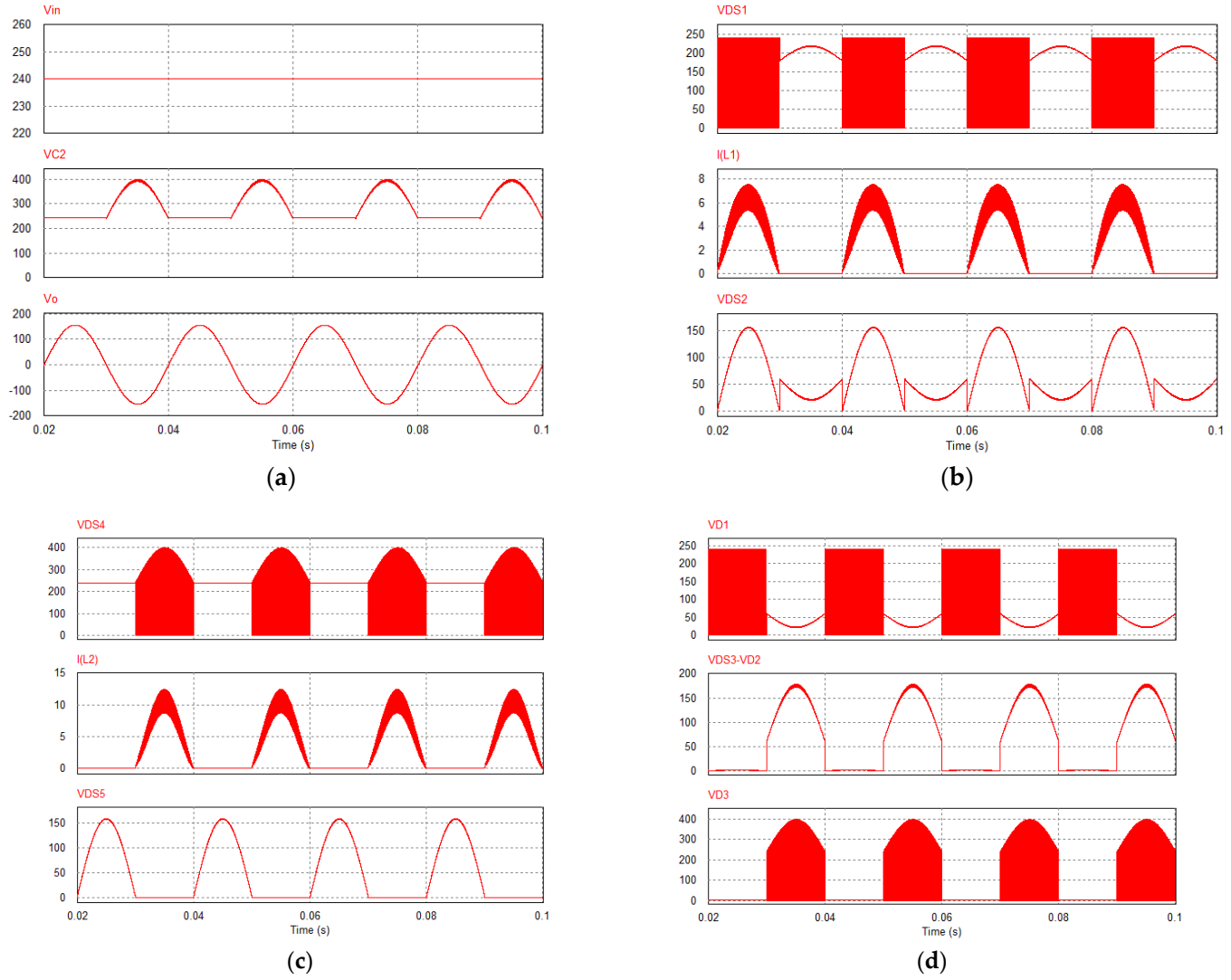

Figure 7. Simulation results with V_{in} = 240 V. (**a**) the input, output and capacitor C_2 voltages, (**b**) the voltage stress on switches S_1, S_2, and the current of inductor L_1, (**c**) the voltage stress on switches S_4, S_5, and the current of inductor L_2, and (**d**) the voltage stress on diodes D_1, D_2, D_3 and the voltage stress on switch S_3.

Moreover, the efficiency of the proposed CGBBI topology was measured at V_{in} = 60 V and V_{in} = 240 V. In this case, the output power of the inverter changed from 25 W to 500 W. When V_{in} = 240 V, the proposed CGBBI topology achieved the highest efficiency of 96.1%. When the input voltage decreased to 60 V, the efficiency of the proposed CGBBI topology also achieved the highest efficiency of 95% at 350 W. From Figure 10, the EU efficiency of the proposed CGBBI topology can be obtained at 95.24%. The parameters for the power losses calculation are presented in Table 4. Figure 11 depicts the power loss distribution of the proposed CGBBI when V_{in} = 60 V and 240 V, v_o = 110 Vrms, and P_o = 500 W.

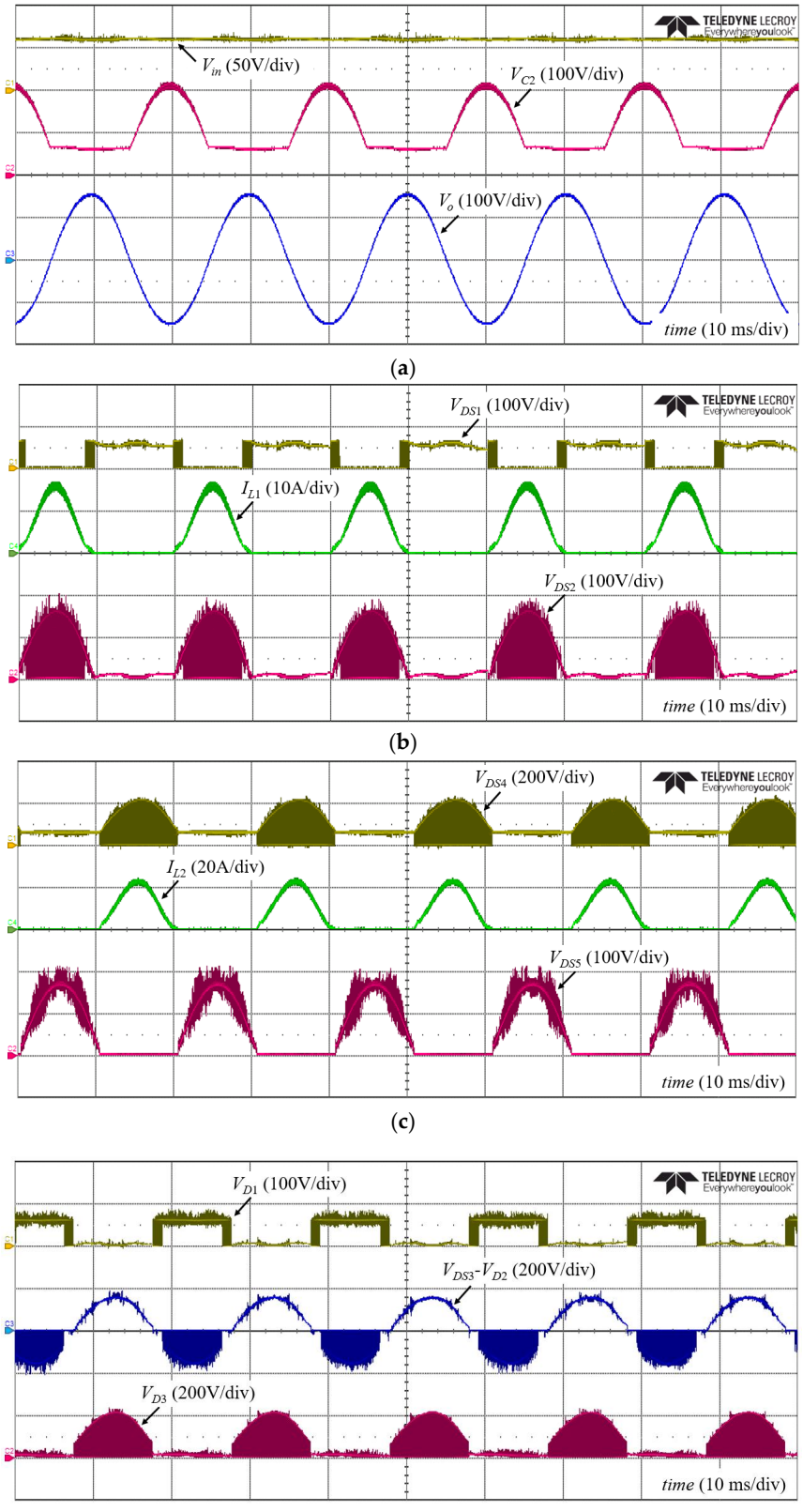

Figure 8. Experimental results with V_{in} = 60 V. (**a**) the input, output and capacitor C_2 voltages, (**b**) the voltage stress on switches S_1, S_2, and the current of inductor L_1, (**c**) the voltage stress on switches S_4, S_5, and the current of inductor L_2, and (**d**) the voltage stress on diodes D_1, D_2, D_3 and the voltage stress on switch S_3.

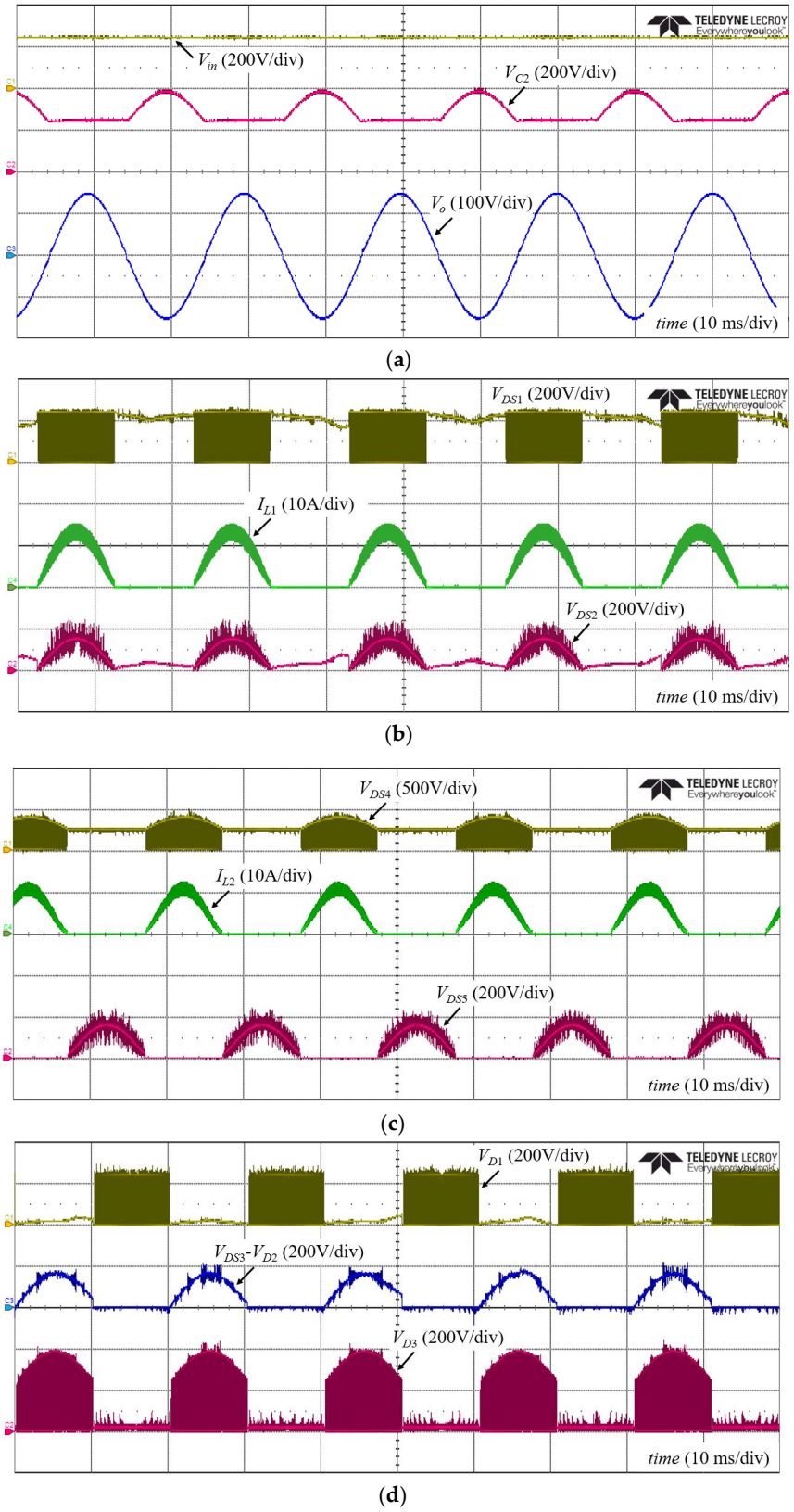

Figure 9. Experimental results with V_{in} = 240 V. (**a**) the input, output and capacitor C_2 voltages, (**b**) the voltage stress on switches S_1, S_2, and the current of inductor L_1, (**c**) the voltage stress on switches S_4, S_5, and the current of inductor L_2, and (**d**) the voltage stress on diodes D_1, D_2, D_3 and the voltage stress on switch S_3.

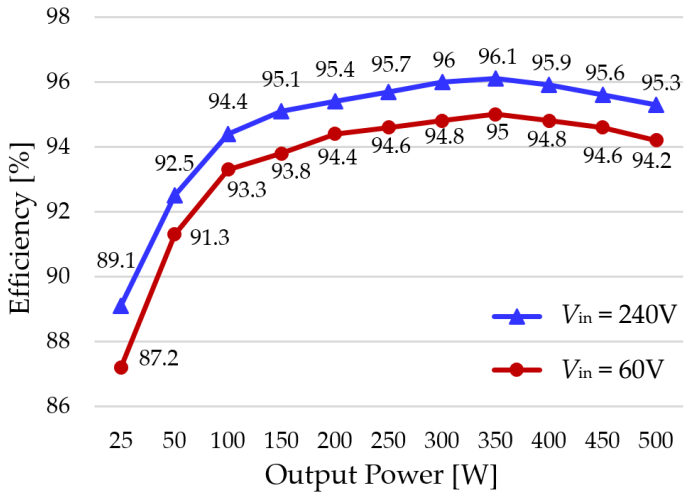

Figure 10. Efficiency measurement with V_{in} = 60 V and V_{in} = 240 V.

Table 4. Parameters for power loss analysis.

Parameters		Values
Inductors L_1, L_2	Core	CM777125 (142 nH/N^2)
	Parastic Resistor	40 mΩ
Capacitors	ESR of C_1	49 mΩ
	ESR of C_2	14 mΩ
MOSFETs		IRFP4668PbF (200 V, 130 A, R_{dson} = 8 mΩ)
		IRFP4868PbF (300 V, 70 A, R_{dson} = 25.5 mΩ)
		IPW60R045CPA (600 V, 60 A, R_{dson} = 45 mΩ)
Diodes		STPS60SM200C (200 V, 30 A, V_F = 0.7 V)
		FF60UP30DN (300 V, 60 A, V_F = 1.12 V)
		DSEI30-06A (600 V, 37 A, V_F = 1.4 V)

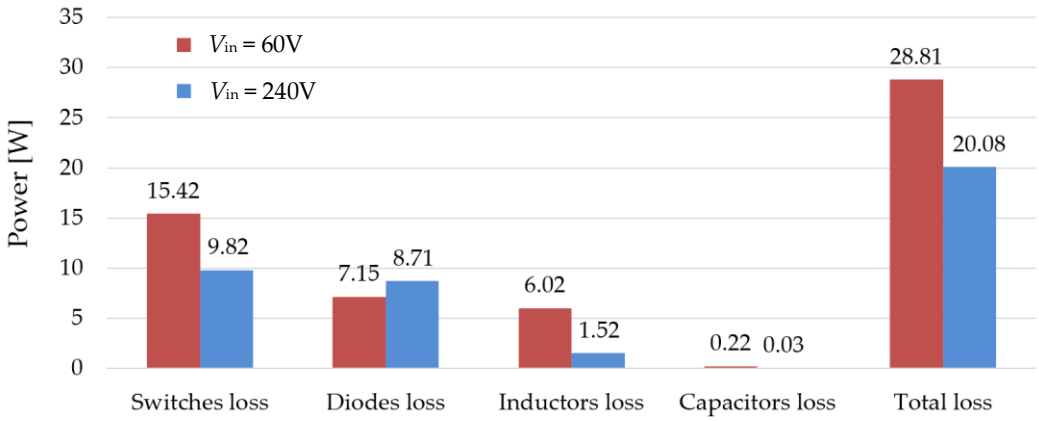

Figure 11. Power loss distribution of the proposed CGBBI.

6. Conclusions

In this article, a common-ground buck–boost inverter topology was introduced, and its theoretical analysis was discussed in detail. In the proposed inverter, there is no common-mode leakage current because the ground of the output side is directly connected to the negative of the DC input power source. The proposed common-ground buck–boost

inverter topology also provides buck–boost capability by controlling the duty cycle of power switches. In addition, few power switches operated with high-switching frequency, so the efficiency of the proposed inverter can be improved. Furthermore, the simulation and experimental verification were presented with a 500 W prototype inverter. The results highlighted that the proposed inverter can steadily operate and have good performance.

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