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# Design and Fabrication of an Isolated Two-Stage AC–DC Power Supply with a 99.50% PF and ZVS for High-Power Density Industrial Applications

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**Abstract:** Power quality in terms of power factor (PF), efficiency, and total harmonic distortions (THDs) is an important consideration in power supplies designed for 5G telecom servers. This paper presents a different magnetic parts design and manufacturing techniques of power supplies, design and selection criteria of switching elements as well as the optimal design of control loops based on small-signal stability modeling and an appropriate stability criterion. The designed telecom power supply consists of the power factor correction (PFC) stage to increase the input power factor and the isolated phase-shift pulse width modulation (PWM) zero-voltage switching (ZVS) DC–DC converter stage to regulate the supply voltage to the specified load value while maintaining a high conversion efficiency. A two-stage outdoor telecom power supply with a power rating of 2 kW was designed and fabricated on a printed circuit board (PCB). The distinct two-stage power components of the power supply were subjected to loss analysis. Furthermore, PSIM simulation and experiments were used to demonstrate the total harmonic distortions (THDs), voltage ripples, power efficiency, and PF performance of the supply current for the proposed power supply under various operating situations. This work produces an industrial high power density power supply with a high PF, low THD and high conversion efficiency which is suitable for telecom power server applications.

**Keywords:** AC-DC power supply; telecom servers; power factor correction (PFC); phase shift PWM DC-DC converter; zero voltage switching (ZVS); small-signal modeling; stability criteria; loss analysis



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## 1. Introduction

The widespread adoption of 5G technology in communications and telecom systems has resulted in the large-scale use of universal electronic devices, which are one of the largest consumers of electrical energy. Because these electronic devices typically operate based on DC power, the AC voltage of the supply must be rectified. Traditional AC–DC rectifiers can be used to power these devices, but their circuit performance and power efficiency in high-power-density applications limit their use [1], so they need to be more energy-efficient. For this reason, a highly efficient AC–DC power supply with a high-power factor has recently been modified [2,3]. Figure 1 shows the overall structure of an AC–DC telecom power supply with two stages, a power factor correction (PFC) stage and a DC–DC output converter stage, which is the optimum option for obtaining a high-power performance and good energy quality [2–4].

The control circuits in the front stage of the high input PF power supply should be implemented to manage the shape of the input AC current waveform to follow the input voltage pure sine waveform. Therefore, the first stage of the two-stage AC–DC power supply is the power factor correction (PFC) stage, which can be implemented with different circuit topologies, such as conventional [5], interleaved [6], and bridgeless [7] ones. Most of these topologies are operated according to the boost converter operation technique, with

voltage and current control loops to control the input current shape and regulate the DC bus voltage to the specified level to supply power to the second stage [8–10].

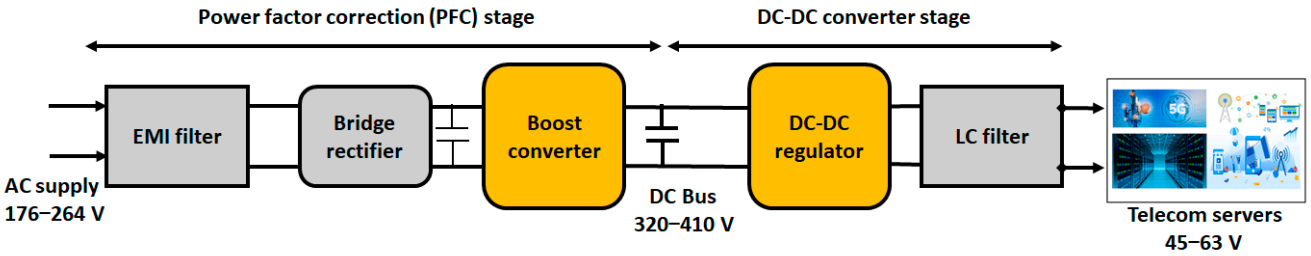



**Figure 1.** The structure of industrial two-stage telecom power supply.

The control loops in PFC converters are typically implemented using proportional-integral (PI) controllers via analog or digital control circuits. In digital PFC converters, the slow dynamic response of the PI controller around the current waveform zero-crossing point in the digital microcontroller unit (MCU) due to the analog-digital conversion (ADC) process increases the displacement and distortion factors of the input current [11]. Thus, more complex modification is required in the current control loop so that the supply current follows the supply voltage and reduces the current zero-crossing distortion, such as the variable on-time switching technique (VOT) [12,13], or implements the digital current filters, such as the finite response impulse (FIR) and the infinite impulse response (IIR) filters [14]. Therefore, analog control circuits with good performance and simple control requirements are preferred and widely used to control industrial PFC converters. To Maintain the specified circuit current and voltage performances, as well as the stability of the designed control systems, the PI controller settings in the control loops of the PFC converters must be optimally acquired. Thus, in the design of the converter's control loops, determining the stability models and selecting the optimal stability requirements of closed-loop control systems in power converters are essential considerations [8,15].

For telecom applications, the second stage of the telecom power supply regulates the DC bus voltage to the desired load voltage (typically 45–63 V) [16]. At this stage, an effective technique for high-power-density conversion with high efficiency must be chosen. The DC–DC converter stage can be constructed as an isolated [17,18] or non-isolated [19] converter depending on the power application. The isolated converter is more extensively used in telecom power applications because it is better suited to provide insulation and protection for connecting loads than the non-isolated converter. In addition, the switching elements on both sides of the high-power-density isolated DC–DC converter must be designed to support high voltage stress on the primary side and high current stress on the secondary side [20,21]. Thus, choosing suitable switching schematics for the converter to reduce the stress on the switches during converter operation is critical in DC–DC converter circuit design.

Isolated DC–DC converters based on the phase-shift PWM switching technique have recently become one of the most widely used techniques due to their ability to reduce switching losses and provide better regulation over a wide load range, particularly when zero-voltage switching (ZVS) operation is available for converter switches [22,23]. ZVS operation enables high-power-density conversion with minimal voltage stress and modest switching losses [24]. Another essential consideration in the design of isolated phase-shift PWM DC–DC converters with ZVS is the transformer design and selection for providing ZVS over a wide load range to minimize switching and conduction losses [25].

According to the preceding discussion, a primary goal when implementing a power supply with a high input PF and high conversion efficiency is to create the appropriate design and optimize the control loops in the PFC converter stage, as well as to design and manufacture power components in both stages of the high-power-density telecom power supply. Thus, this paper proposes optimal design analysis and implementation of the PFC converter stage voltage and current control loops based on the derived small-signal model

and appropriate stability criteria that maintain the supply current and voltage in phase in order to develop an industrial two-stage high-power-density telecom power supply with a high input PF, a lower THD, and high conversion efficiency. Optimal mathematical analysis, selection methodology, and manufacturing techniques for magnetic and switching parts to withstand high voltage and current stresses while consuming little power are presented. Additionally, losses in various parts of the power supply are analyzed and calculated.

The remainder of this paper is arranged as follows: Section 2 delves into the design approach, manufacturing procedures, and loss analysis of the PFC converter stage power components. An optimal control technique for control loops of the PFC converter stage is also proposed. The optimal design technique and loss analysis of the isolated phase-shift ZVS PWM DC–DC converter stage are presented in Section 3. The simulation approach and results for the overall designed two-stage AC–DC power supply are presented in Section 4. Section 5 depicts the printed circuit board (PCB) design, experimental verification, and comparative analysis of the simulation, as well as experimental and analytical performance for the designed AC–DC power supply. The last section of the paper presents the conclusions.

## 2. Power Factor Correction (PFC) Stage Design

For the PFC converters implemented for the high-power density, the conventional, interleaved or bridgeless topology can be used. The bridgeless PFC typologies have higher efficiency compared to the other PFC topologies since the input bridge rectifier is not used. However, most of these bridgeless topologies experience a higher level of EMI due to the direct connection between the input supply and the DC power circuit which increases the THD and reduced the PF. Different modifications of bridgeless topologies with complex designs and higher costs of the required EMI filters have to be implemented to decrease these EMI issues [7]. Therefore, the use of the bridgeless PFC topology is limited in telecom power applications with high power density, where the EMI level is required to be at a lower limit. In addition, the interleaved PFC converter can reduce the input ripple current as compared with the conventional PFC topology due to the interleaving technique which causes the ripple current cancellation, reduces THD, and increases the input PF to about 99.90%; however, the control circuit and price are higher than the conventional PFC with little difference in the performance [6,8].

On the other hand, the conventional PFC is a simple topology that can be implemented with economical features to work in high power density applications with a higher efficiency of more than 97%, a higher PF of more than 99% and a lower THD [8]. Therefore, in this work, the conventional PFC converter based on the single-phase boost converter is selected to implement the front stage of the designed two-stage AC-DC power supply.

Figure 2 shows the employed conventional boost PFC stage designed for the two-stage AC–DC telecom power supply. As shown in the circuit schematic, the principal operation of the circuit is based on the single-phase boost converter operation technique. In the boost converters, the three main power elements to be optimally designed are (1) the energy storage element represented by the boost inductor ($L_b$), (2) the switching parts represented by the high-voltage Mosfet ($Q_b$) and the high current fast switching diode ($D_b$), and (3) the output filter represented by the DC bus capacitor ($C_b$).

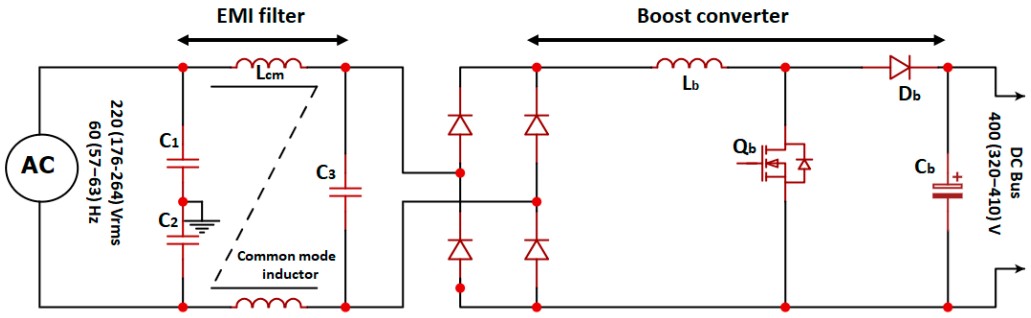



**Figure 2.** Schematic circuit of the employed telecom PFC stage.

Table 1 presents the design specifications of the two-stage AC–DC 5G telecom power supply based on the design requirements of the LGU$^+$ telecom company for the 5G telecom power servers.

**Table 1.** The target PFC converter stage design specifications.

| Design Parameter | Value | Unit |
|---|---|---|
| Operating voltage ($V_s$) | 220 (176–264) | V |
| Operating Frequency ($F_s$) | 60 (57–63) | Hz |
| DC bus Voltage ($V_{bus}$) | 400 (320–410) | V |
| Rated Power ($P_o$) | 2000 | W |
| Target Efficiency ($\eta$) | 97% | - |
| Target power factor (PF) | 99% | - |
| PFC Switching Frequency ($F_{sw}$) | 100 | kHz |
| Hold Up Time ($t_{hu}$) | 6 | ms |
| Inductor ripple current (%*Ripple*) | 15% | - |
| DC bus voltage ripple ($V_{rpp}$) | 15 | $V_{pp}$ |

### *2.1. PFC Stage Power Components Design and Manufacturing*

#### 2.1.1. Boost Inductor

When choosing boost inductors for high-power-density PFC boost converters, various factors must be considered, including the required inductance value, the direct current resistance (DCR), and the saturation current value. It is necessary to select a suitable inductor core with small core losses, calculate the number of turns that provide the required inductance value, and design the inductor wire that withstands the peak value of the current that flows through the inductor with acceptable power losses due to wire DCR value. Therefore, the design and manufacturing procedure of the boost inductor is as follows:

1. The required boost inductance value can be obtained on the basis of the required boost inductor input ripple current, which is commonly computed as a percentage (10–40%) of the maximum input current to the boost converter. As given in the design specifications in Table 1, for a 15% ripple current, the inductor ripple current can be calculated as

$$I_{L\ ripple} = 0.15 \times I_{in\ max} \tag{1}$$

where $I_{in\ max}$ is the boost converter maximum input current and can be calculated as

$$I_{in\ max} = \sqrt{2} \times \frac{P_o}{\eta \times V_{in\ min} \times PF} \tag{2}$$

where $V_{in\ min}$ is the minimum input voltage to the boost converter in V. η and PF are the target efficiency and power factor of the designed PFC stage, respectively.

Using Equations (1) and (2), the allowable ripple inductor current at full loading can be calculated. The boost inductor minimum value is calculated on the basis of this ripple current value and 0.5 of the value of the worst-case scenario of the boost converter duty cycle (D), as given below:

$$L_{b\ min} = \frac{V_{bus} \times D(1-D)}{F_{sw} \times I_{L\ ripple}} \tag{3}$$

where $F_{sw}$ is the switching frequency in Hz and $V_{bus}$ is the DC bus voltage in V.

2. To compute the average and maximum peak currents of the specified boost inductor, the boost converter used is assumed to work in the continuous current conduction mode (CCM), with two operation modes when the switch $Q_b$ is on and off. Figure 3 depicts the boost converter's inductor voltage and current waveforms in various operation modes.

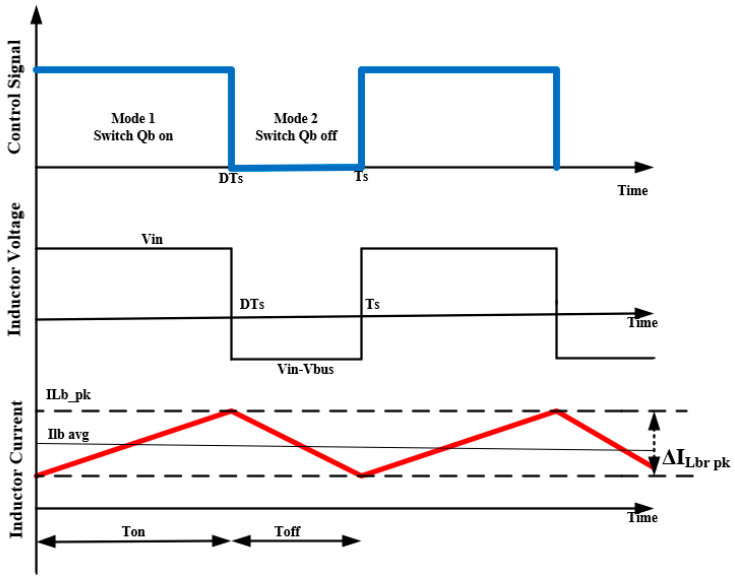



**Figure 3.** Boost inductor voltage and currents waveforms of the employed PFC topology.

When the switch ($Q_b$) is closed in **Mode 1**, the energy is stored in the inductor and a magnetic field is generated. When $Q_b$ is opened in **Mode 2**, the current circuit impedance rises, lowering the current, and the magnetic field previously created is reduced, allowing the current to flow toward the load. As a result, the inductor voltage polarity is reversed, putting the two sources in series and charging the DC bus capacitor ($C_b$) via the fast-switching diode ($D_b$).

The inductor maximum average current ($I_{Lb\ avg\ max}$) can be calculated at the rated power condition ($P_o$), the rated $V_{bus}$, and the minimum operating duty cycle ($D_{PFC\ min}$) as given below:

$$I_{Lb\ avg\ max} = \frac{P_o}{V_{bus}}\left(\frac{1}{1 - D_{PFC\ min}}\right) \tag{4}$$

As shown in Table 1, the boost converter is designed to work with a wide supply voltage range (176–264) V. So, the PFC stage minimum duty cycle value can be calculated as

$$D_{PFC\ min} = 1 - \frac{V_{in\_max}}{V_{bus}} \tag{5}$$

The inductor ripple current $I_{Lbr\ pk}$ as the percentage ($\%Ripple$) of the boost converter total input current can be expressed as

$$I_{Lbr\ pk} = \%Ripple \times I_{Lb\ avg\ max} \times 2 \tag{6}$$

Therefore, the inductor maximum peak current is calculated as

$$I_{Lb\ pk} = I_{Lb\ avg\ max} + \frac{I_{Lbr\ pk}}{2} \tag{7}$$

3. On the basis of the calculated inductance and the inductor maximum peak current, the inductor core part number, the number of turns ($N$), and the size of the winding wire have to be selected.

The boost converter inductor core was designed to have a high saturation level, which prevents saturation at the maximum peak current ($I_{L\ pk}$) and supports the converter operation with the designed switching frequency. The inductor core losses also have to be accepted in accordance with the temperature rise during the PFC converter operation. Therefore, Kool Mμ core materials, with low loss, a relatively high saturation level (10,500 gausses), a higher switching frequency level (up to 200 kHz), and near-zero mag-

netostriction (ability to expand or contract in response to a magnetic field), are good for eliminating audible frequency noise in in-line noise filters and inductors and also excellent for implementation in PFC circuits [26].

As depicted in Figure 4 chart, the inductor core in this work will be chosen by the $LI^2$ method. The core part number will be chosen from the Kool Mu chart of the Magnetic inc supplier [27], where L is the boost inductance value and I is the inductor maximum peak current.

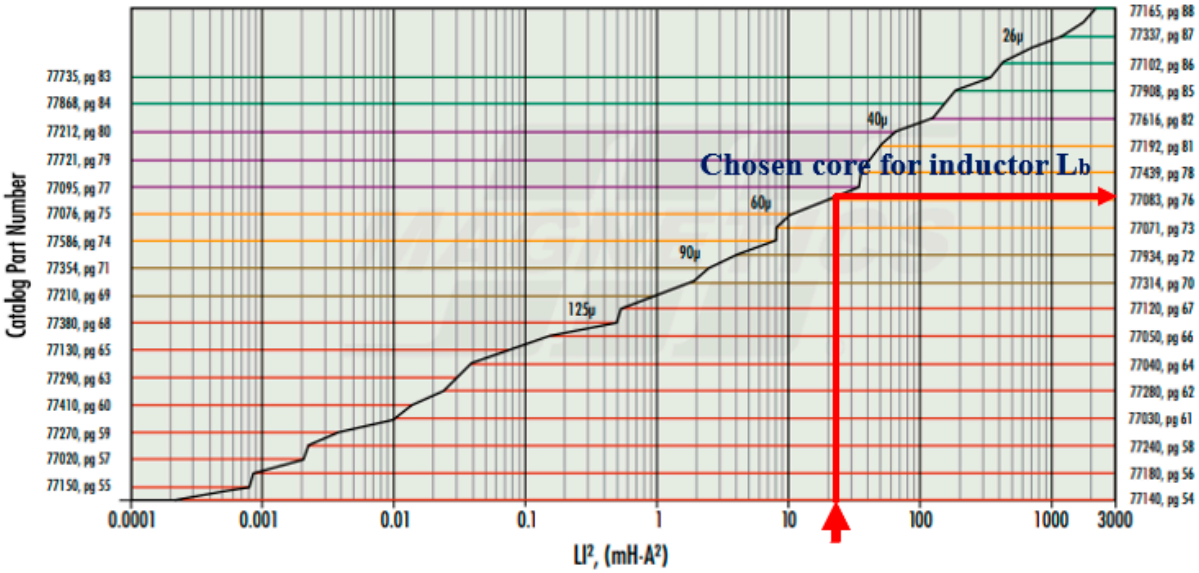



**Figure 4.** Kool Mμ chart for choosing the $L_b$ inductor core for the PFC boost converter.

Using the calculated value of $LI^2$ and the required inductance value from the chart and ensuring suitable space for the wire to wind around the core, the boost converter inductor is designed using two stacked Kool Mμ toroids core with part number 77083A7. The number of turns ($N_{Lb}$) in the inductor to obtain the required inductance value ($L_b$) can be calculated as

$$N_{Lb} = \sqrt{\frac{L_b}{2\,A_{L\_min}}} \tag{8}$$

where $A_{L\_min}$ is the minimum inductance factor for each core.

The inductor wire is chosen on the basis of the maximum peak current of the inductor and must be thick enough to keep the DCR low and be able to form the appropriate number of turns around the selected core area.

4. Power losses in the PFC boost inductors are caused by (i) the *DCR* resistance losses ($P_{Lb\ DCR}$) of the inductor wire and (2) the inductor core losses ($P_{Lb\ Core}$).

The *DCR* losses of the boost converter inductor ($P_{Lb\ DCR}$) can be calculated as

$$P_{Lb\ DCR} = {I_{Lb\ rms}}^2 \times DCR \tag{9}$$

where the designed inductor *DCR* value can be experimentally measured by applying DC current and voltage to the terminal of the inductor and using Ohm's law to obtain the equivalent inductor terminal resistance and $I_{Lb\ RMS}$ is the inductor maximum RMS current and can be calculated as

$$I_{Lb\ rms} = \frac{P_o}{\eta \times V_{in\_min} \times PF} \tag{10}$$

On the basis of the supplier of the chosen core, the core losses of the inductor ($P_{Lb\ Core}$) can be directly obtained from the core datasheet or calculated using the given equation:

$$P_{Lb\ core} = K_1 \times F_{sw}^{x} \times B^{y} \times V_e \times 10^{-3} \tag{11}$$

where $K_1$ is constant for the core material, $x$ is the frequency exponential, $B$ is the peak flux density in Gauss, y is the flux density exponential, and $V_e$ is the effective core volume in $cm^3$.

In this work, and based on the design analysis, the boost inductor was manufactured with 60 turns of 1.15 mm copper wire wrapped around the 2-stacked Kool Mμ 77083A7 toroid cores. The *DCR* value of the manufactured inductor was measured experimentally and found to be around 0.087 Ω. The electrical specifications of the designed boost inductor are summarized in Table 2.

**Table 2.** Electrical specifications of the designed boost inductor ($L_b$).

| Parameter | Value |
|---|---|
| Actual inductance | 470 uF |
| Peak current | 11.60 A |
| Core type | 2 stacked Kool Mμ (77083A7) |
| Inductive factor ($A_L$) | 81 ± 8% ($nH/T^2$) |
| No. of Turns ($N_{Lb}$) | 60 |
| Winding wire | Copper 1.15 mm |
| DC resistance (DCR) | 0.087 Ω |

#### 2.1.2. DC Bus Capacitor

When selecting the output bulk capacitor ($C_b$) for a PFC boost converter, it is critical to keep the equivalent series resistance (*ESR*) as low as possible because it affects power efficiency and voltage regulation. A higher ESR causes more ripples, influencing the stability of the boost converter control loop [28]. Typically, aluminum electrolytic capacitors are used, which require a high-power density; moreover, due to their small volume, these capacitors are also preferred in PFC applications because they provide a high capacitance value with a low *ESR*.

The DC bus capacitor for PFC boost converters is typically designed with a value that must meet the specified DC bus voltage ripple (*Vrpp*) using Equation (12) and be sufficient to deliver the output minimum voltage hold-up with the specified time ($t_{hu}$), as given in Equation (13).

$$C_b \geq \frac{P_o}{2 \times \pi \times F_{min} \times V_{rpp} \times V_{bus}} \tag{12}$$

$$C_b \geq \frac{2 \times P_o \times t_{hu}}{\eta (V_{bus}^2 - V_{bus\ min}^2)} \tag{13}$$

The output capacitor was designed using the larger of the two equations.

The capacitor RMS current ($I_{Cb\ RMS}$) across the 60 Hz line cycle is given as [29]

$$I_{Cb\ rms} = \sqrt{\left( \frac{8\sqrt{2} \times P_o^2}{3\pi \times V_{in\_min} \times V_{bus}} - \frac{P_o^2}{V_o^2} \right)} \tag{14}$$

The capacitor equivalent series resistance (*ESR*) is calculated on the basis of the dissipation factor (*DF*) of the chosen DC bus capacitor $C_b$ at the low line frequency as

$$ESR = \frac{DF}{2 \times \pi \times F \times C_b} \tag{15}$$

The ESR losses of the DC bus capacitor $P_{Cb\ ESR}$ can be calculated as

$$P_{Cb\ ESR} = ESR \times I_{Cb\_rms}^2 \tag{16}$$

To reduce the equivalent ESR of the DC bus capacitor to reduce the power losses, the calculated capacitance value can be divided into n number of capacitors in parallel. In this work, the largest value of the DC bulk capacitor, calculated using Equation (12), was about

950 uF. So, two capacitors of 560 uF and 450 V, with a low ESR value, are used in parallel to reduce the effective ESR value and hence reduce the capacitor losses. The dissipation factor of the chosen capacitor is about 0.15, so the capacitor ESR is calculated to be about 0.355 Ω.

#### 2.1.3. Mosfet Switch

To choose an optimal Mosfet ($Q_b$) for a boost converter implemented for PFC converters, there are some important Mosfet selection considerations, which can be summarized as follows: low on-state resistance ($R_{dson}$) for low power losses, fast turn-on/off switching to reduce device switching losses, low output capacitances to increase efficiency with light load conditions, high $dV_{DS}/dt$ and high $dI_F/dt$ to withstand the spikes and overshoots, and low thermal resistance to decrease thermal power dissipation [1,30,31].

To minimize conduction losses, the power Mosfet switches in PFC boost converters are chosen on the basis of the highest peak current considering the value of the on-state drain–source resistance ($Rds_{on}$). The RMS current ($I_{Qb\ RMS}$) and the highest peak current stress ($I_{Qb\ pk}$) in the boost converter switch $Q_b$ can be calculated as [8]

$$I_{Qb\ rms} = \frac{P_o}{V_{in\ min}}\sqrt{1 - \frac{8\sqrt{2}V_{in\ min}}{3\pi V_{bus}}} \tag{17}$$

$$I_{Qb\ pk} = \sqrt{2} \times I_{Qb\ rms} \tag{18}$$

In this work, considering the calculated switch's highest peak current, the maximum output voltage ratings, the low switch *Rdson*, and the IPZ60R040C7 switch is used for the PFC stage. The $Rds_{on}$ of the chosen switch is about 40 mΩ.

The power losses in the Mosfet switch are classified into two parts, the conduction losses ($P_{Qb\ Rdson}$) due to the on-state resistance and the switching losses ($P_{Qb\ sw}$).

The conduction losses ($P_{Qb\ Rdson}$) of the switches can be estimated as:

$$P_{Qb\ Rdson} = I^2_{Qb\ rms} \times Rds_{on} \tag{19}$$

For the chosen Mosfet switch, the output capacitance $C_{oss}$ = 85 pf, the rise time $t_r$ = 8 ns, and the fall time $t_f$ = 0.2 ns of the Mosfet gate. Using these values, switching losses and losses due to the output capacitance ($P_{Qb\ sw}$) can be determined as

$$P_{Qb\ sw} = F_{sw}\left[0.5 \times V_{bus} \times I_{in\ pk} \times \left(t_r + t_f\right) + 0.5 \times C_{oss} \times V^2_{bus}\right] \tag{20}$$

#### 2.1.4. Boost Diode

In PFC boost converters, the boost diode ($D_b$) has a big influence on the system's performance due to the reverse recovery behavior. So, an ultra-fast diode with a low reverse recovery time ($t_{rr}$) and reverse recovery charge ($Q_{rr}$) is necessary to reduce the switching loss.

The boost diode peak current is calculated as the maximum load current at the minimum DC bus voltage, as follows:

$$I_{Db\ pk} = \frac{P_{out}}{V_{bus\ min}} \tag{21}$$

The diode losses $P_{Db\ loss}$ are estimated on the basis of the forward voltage ($V_f$) at 125 °C and the reverse recovery charge ($Q_{rr}$) of the diode.

$$P_{Db\ Loss} = V_f \times I_{Db\ pk} + 0.5 \times F_{sw} \times V_{bus} \times Q_{rr} \tag{22}$$

In this work, the silicon carbide (SiC) Schottky diode (with new diode technology) with part number IDH16G65C5 with a forward voltage of about 1.5 V and no reverse recovery/no forward recovery is used as the boost diode. As a result, the switching

loss caused by this diode can be ignored and only the conductivity loss caused by $V_f$ is considered.

### 2.2. Power Loss Distribution in the PFC Stage

Table 3 summarizes the design procedure results of the power components and power loss calculations in the employed PFC converter stage. Figure 5 depicts the loss distribution in the PFC stage power components. In the input bridge rectifier, the total power losses amount to about 36%, followed by the power losses in the boost inductor, by 30%, and the expected conversion efficiency, which is calculated from the proposed optimal design analysis of the designed PFC stage, is about 97.10%.

**Table 3.** Design components and losses of the employed PFC stage.

| Component | Quant. | Part Number/Description | Power Loss (W) | Efficiency |
|---|---|---|---|---|
| Bridge rectifier | 2 | GSIB 2580 | 21.32 | 97.10% |
| Boost inductor $L_b$ | 1 | Core: (2 stacked cores Kool Mμ (77083A7). Single 1.15 Copper wire 60 Turns | 17.12 | |
| Mosfet $Q_b$ | 1 | IPZ60R040C7 | 6.85 | |
| Diode $D_b$ | 1 | IDH16G65C5 | 9.375 | |
| DC bus capacitor $C_b$ | 2 | EKMR421VSN561MR50S | 3.90 | |

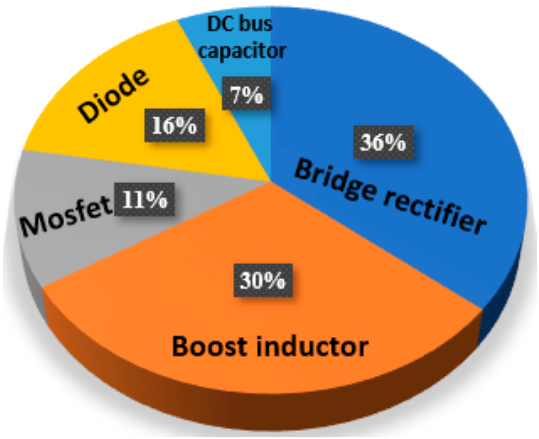



**Figure 5.** Power losses distribution in PFC stage.

### 2.3. Boost Converter Average Small-Signal Model

Assuming that the single-phase boost converter unit employed in this work, as shown in Figure 6, is working in the continuous current conduction (CCM) mode, the mathematical equations that describe the change in the inductor current ($I_{Lb}$) and the DC bus voltage ($V_{bus} = V_o$) can be given as

$$\frac{dI_{Lb}}{dt} = \frac{V_{in}}{L_b} - \frac{V_{bus}(1-D)}{L_b} \tag{23}$$

$$\frac{dV_{bus}}{dt} = -\frac{V_{bus}}{R\,C_b} + \frac{I_{Lb}(1-D)}{C_b} \tag{24}$$

where $D$ is the PFC boost converter duty cycle and $R$ is the load resistance in Ohms.

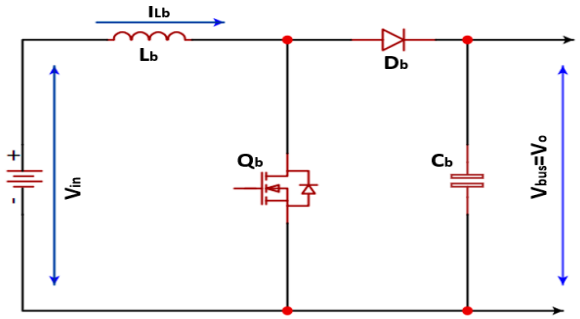



**Figure 6.** Equivalent circuit of the boost converter unit.

We assume that at the selected operational points ($i_{Lb}$, $v_{in}$, $v_{bus}$, and $d$), all variables ($I_{Lb}$, $V_{in}$, $V_{bus}$, and $D$) are in a steady state when the AC signal variation is small ($i_{Lb}$*, $v_{in}$*, $v_{bus}$*, and $d$*), where

$$I_{Lb} = i_{Lb} + i_{Lb}^{*}\ ;\ V_{in} = v_{in} + v_{in}^{*}\ ;\ V_{bus} = v_{bus} + v_{bus}^{*}\ ;\ D = d + d^{*} \tag{25}$$

To regulate the DC bus voltage ($V_{bus}$) and boost the inductor current ($I_{Lb}$), the designed control system must modify the duty cycle ($D$) on the basis of the variation in the small-signal AC.

Equations (26) and (27) are obtained by substituting values from Equation (25) in Equations (23) and (24).

$$\frac{d\left(i_{Lb} + i_{Lb}^{*}\right)}{dt} = \frac{\left(v_{in} + v_{in}^{*}\right)}{L_b} - \frac{\left(v_{bus} + v_{bus}^{*}\right)\left(1 - d - d^{*}\right)}{L_b} \tag{26}$$

$$\frac{d\left(v_{bus} + v_{bus}^{*}\right)}{dt} = -\frac{\left(v_{bus} + v_{bus}^{*}\right)}{R\,C_b} + \frac{\left(i_{Lb} + i_{Lb}^{*}\right)\left(1 - d - d^{*}\right)}{C_b} \tag{27}$$

Using the averaging model, which considers that over the switching period in the steady state the inductor current change and the capacitor voltage change are zero, Equations (26) and (27) can be rewritten as

$$\frac{d\left(i_{Lb}^{*}\right)}{dt} = \frac{1}{L_b}\left(v_{in}^{*}\right) + \frac{v_{bus}}{L_b}\left(d^{*}\right) - \frac{(1-d)}{L_b}\left(v_{bus}^{*}\right) \tag{28}$$

$$\frac{d\left(v_{bus}^{*}\right)}{dt} = \frac{(1-d)}{C_b}\left(i_{Lb}^{*}\right) + \frac{i_{Lb}}{C_b}\left(d^{*}\right) - \frac{1}{R\,C_b}\left(v_{bus}^{*}\right) \tag{29}$$

Using Equations (28) and (29), the small-signal stability model for the bridge CCM PFC converter in the state space matrix is as follows:

$$\begin{bmatrix} i_{Lb}^{*} \\ v_{bus}^{*} \end{bmatrix} = \begin{bmatrix} 0 & -\left(\frac{1-d}{L_b}\right) \\ \left(\frac{1-d}{C_b}\right) & \frac{-1}{R\,C_b} \end{bmatrix} \begin{bmatrix} i_{Lb}^{*} \\ v_{bus}^{*} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} & \frac{V_{bus}}{L_b} \\ 0 & \frac{i_{Lb}}{C_b} \end{bmatrix} \begin{bmatrix} v_{in}^{*} \\ d^{*} \end{bmatrix} \tag{30}$$

### *2.4. PFC Stage Control Circuit Design*

Figure 7 shows the implementation of the control circuit for the boost converter, which consists of the outer voltage control loop to regulate the DC bus voltage and the inner current control loop to control the inductor current shape in order to allow the input supply current to follow the supply voltage for the high input power factor. The sensed DC bus voltage ($V_{bus\_fb}$) is compared with the reference DC voltage ($V_{ref}$) to generate the DC error, which controls using a PI controller and then shapes with the sensed input voltage ($V_{in\_fb}$) to generate the reference current for the inner current control loop.

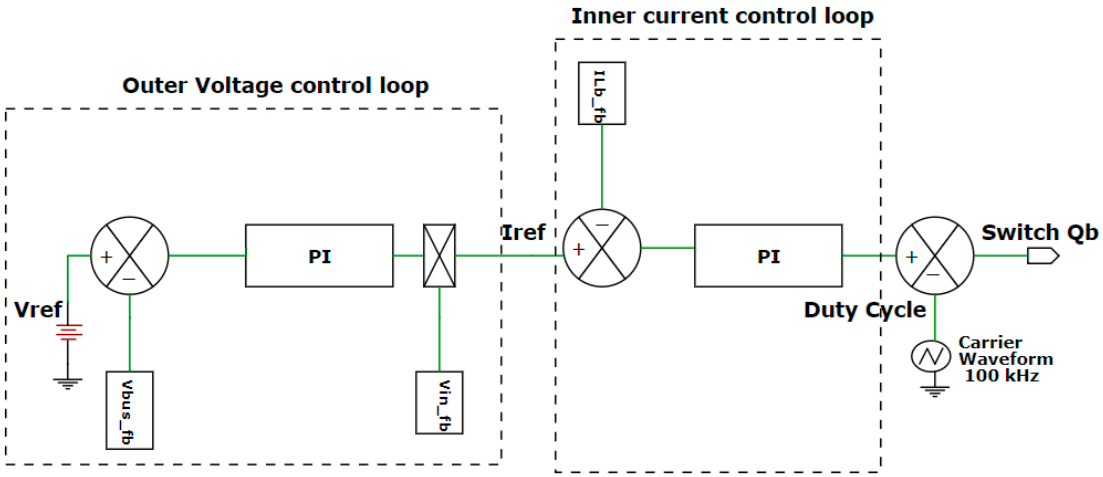



**Figure 7.** Control loop of the employed PFC boost converter.

A Laplace transform is applied for the small-signal stability model of the PFC converter obtained in Equation (30) to obtain the open loop transfer functions for the DC bus voltage and the inductor current control systems, as follows:

$$G_v(s) = \frac{v^*_{bus}(s)}{i^*_{Lb}(s)} = \frac{V_{in}}{2\,V_{bus}\,C_b s} \tag{31}$$

$$G_i(s) = \frac{i^*_{Lb}(s)}{d^*(s)} = \frac{\frac{V_{bus}}{L_b}\,s + \frac{2V_{bus}}{L_b R C_b}}{s^2 + \frac{1}{C_b R}\,s + \frac{1}{L_b C_b}(1-d)^2} \tag{32}$$

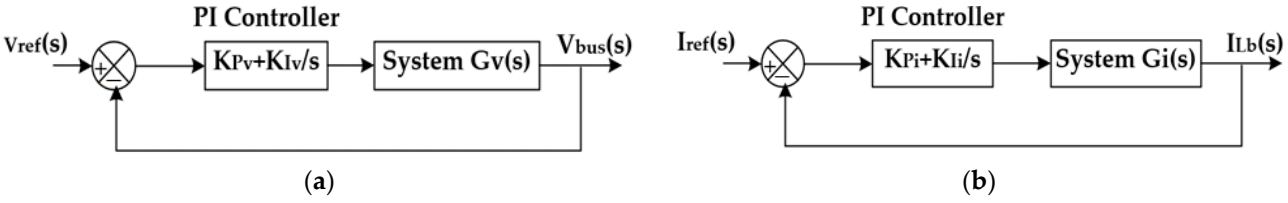
At a high switching frequency, the DC bus capacitor can be shorted and $1/C_b$ is equal to zero, which can simplify the inductor current open loop TF as given below:

$$G_i(s) \cong \frac{V_{bus}}{sL_b} \tag{33}$$

Figure 8 shows the block presentation of the closed loop TF in the voltage and current control loops of the boost converter of the PFC stage, where the closed loop TF of the outer voltage $G_{CLv}(s)$ and inductor current $G_{CLi}(s)$ control systems can be expressed as

$$G_{CLv}(s) = \frac{V_{bus}(s)}{V_{ref}(s)} = \frac{\frac{V_{in}}{2\,V_{bus}\,C_b}.(K_{Pv}\,s + K_{Iv})}{s^2 + \frac{V_{in}\,K_{Pv}}{2\,V_{bus}\,C_b}s + \frac{V_{in}\,K_{Iv}}{2\,V_{bus}\,C_b}} \tag{34}$$

$$G_{CLi}(s) = \frac{I_{Lb}(s)}{I_{ref}(s)} = \frac{\frac{V_{bus}}{L_b}.(K_{Pi}\,s + K_{Ii})}{s^2 + \frac{V_{bus}\,K_{Pi}}{L_b}s + \frac{V_{bus}\,K_{Ii}}{L_b}} \tag{35}$$




(**a**) (**b**)

**Figure 8.** Closed control loops of the PFC boost converter: (**a**) voltage loop; (**b**) current loop.

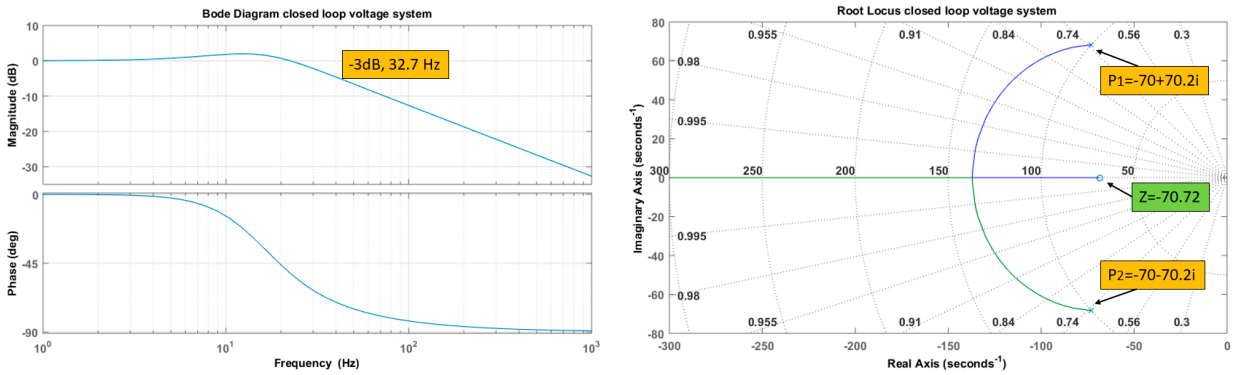
After the transfer functions of the control loops are determined, the PI controllers' gains can be designed with the standard form of the second-order system TF and bode plots by selecting the proper control system bandwidth and the undamped natural frequency

that enhanced the optimal stability criteria for the closed loop of the voltage and current control systems.

Usually, the bandwidth of the outer voltage loop must be significantly small in order to eliminate the harmonics of the output DC voltage reflected by the AC input voltage at 60 Hz. On the contrary, the bandwidth of the inner current control loop must be significantly high compared with the voltage control loops to allow the inductor's current to follow the reference current. In addition, the current control loop bandwidth must be less than the switching frequency ($F_{sw}$) to reject the noise at the switching frequency [8,32].

In this work, the undamped natural frequency (ξ) was considered to be about 0.707 and the closed loop bandwidths of $W_n$ were assumed to be about 100 rad/s and 10 krad/s for the outer voltage and inner current loops, respectively. For the reliable operation of a controller under different loading conditions, the $Kp$ and $K_I$ parameters were set to work with the minimum value of the load voltage ($V_{bus}$) of 320 V with the rated input voltage.

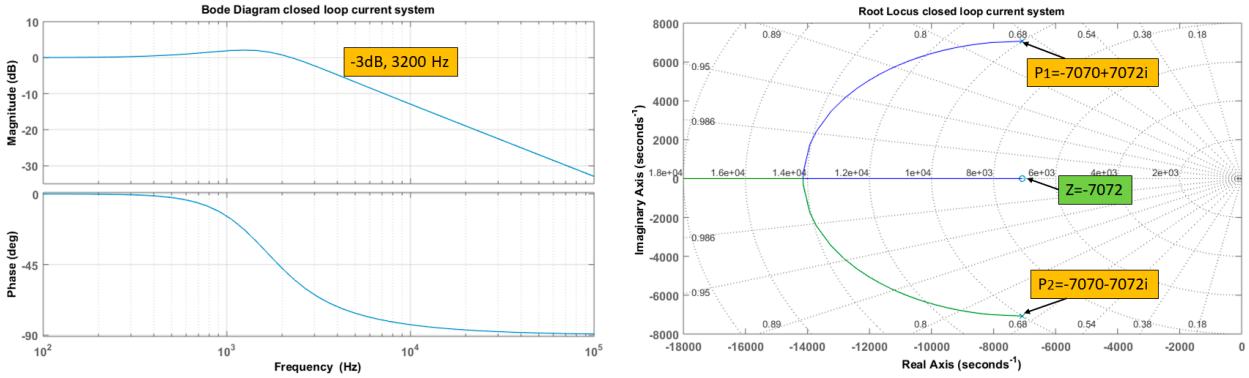
Figure 9 depicts the bode plot of the frequency response of the closed loop voltage control system, which shows that the voltage controller offers unity gain for frequencies less than 32.7 Hz. This voltage controller works as a low-pass filter to remove the 60 Hz voltage ripple. In addition, the root locus plot of the pole-zero location, which shows the designed voltage control poles and zeros located on the left and the designed voltage controller, is inherently stable.




(**a**) (**b**)

**Figure 9.** Closed loop voltage control system characteristics (**a**) bode plot; (**b**) root locus plot.

Figure 10 depicts the bode plot of the frequency response of the closed loop current control system, which shows that the current controller offers unity gain for frequencies less than 3200 Hz. This current control system, working as a low-pass filter, helps to remove the switching frequency noise. Moreover, the root locus plot of the pole-zero location, which shows the designed current control poles and zeros located on the left and the designed current controller, is also inherently stable.




(**a**) (**b**)

**Figure 10.** Closed loop current control system characteristics (**a**) bode plot; (**b**) root locus plot.

## 3. Phase-Shift PWM ZVS DC–DC Converter Stage Design

Figure 11 shows the schematic circuit of the telecom phase-shift PWM ZVS DC–DC converter stage, consisting of three main parts: (1) the full bridge switching circuit on the primary side with phase-shift PWM and ZVS technique, which involves tuning the resonant inductor $L_r$ to exhaust the energy of the parasitic capacitance of the switches at the moment of the switching, which offers current flow with zero voltage biasing, reducing switching losses and increasing the conversion efficiency, (2) the synchronous rectifier on the secondary side, which uses power Mosfets to rectify the output voltage of the HF transformer, and (3) the output LC filter to adjust the load voltage and current ripple contents and maintain the output voltage hold-up time at the specified values.

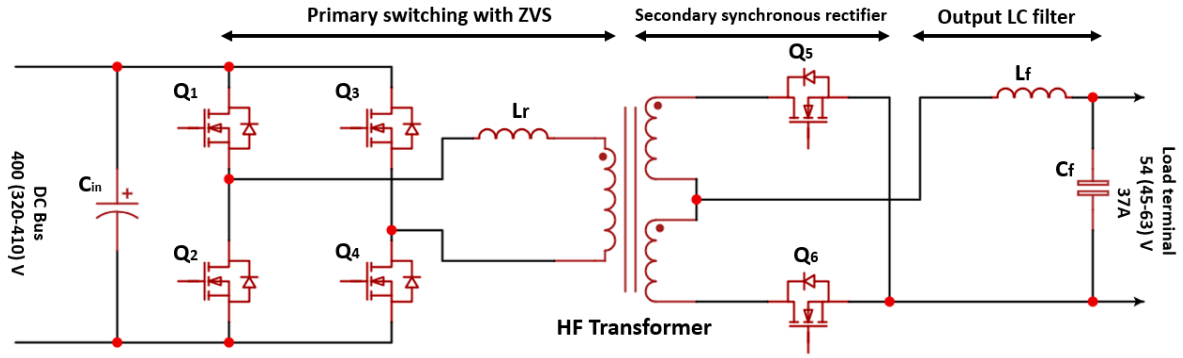



**Figure 11.** Schematic circuit of the employed phase shift PWM ZVS DC-DC converter.

Challenges in designing high-power-density ZVS converters are (1) selecting primary Mosfets to withstand the high DC voltage on the input side with small conduction losses, (2) designing a resonant inductor that offers ZVS over a wide range of loading conditions, (3) selecting secondary Mosfets to withstand the high load current with small conduction and switching losses, and (4) tuning the output filter components to adjust the load voltage and current ripple components. The following sections present the design consideration, mathematical calculation, and loss analysis of the DC–DC converter stage of different power components.

Table 4 shows the design specifications of the employed phase-shift PWM ZVS DC–DC converter based on the LCU$^+$ telecom company for the 5G telecom power servers.

**Table 4.** Design specifications of the employed DC–DC converter stage.

| Parameter | Value | Unit |
|---|---|---|
| Input voltage ($V_{bus}$) | 400 (320–410) | V |
| Load voltage ($V_{load}$) | 54 (45–63) | V |
| Output voltage ripple | 200 | mV |
| Rated power ($P_{load}$) | 2000 | W |
| Switching frequency | 100 | kHz |
| Target efficiency | 95% | |
| holdup time ($t_{hold}$) | 20 | us |
| Inductor ripple current | 15% | |

### *3.1. Phase-Shift PWM ZVS Converter Power Component Design and Manufacture*

#### 3.1.1. High-Frequency (HF) Transformer

Key parameters to be considered in the design of high-frequency transformers for DC–DC converters are as follows: effective (operating) duty cycle to calculate the transformer turn ratio; the magnetization inductance to realize ZVS; the shape, size, and material of the transformer core that reduce the oscillations; the number of magnets; elimination of eddy currents; and high dv/dt to withstand the overshoots and high voltage stress on the primary side [25,33–35]. Therefore, the design and manufacturing procedure of high-

frequency transformers for high-power-density DC–DC converters can be summarized as follows:

1. The transformer turns ratio (a) is calculated on the basis of the maximum operating duty cycle ($D_{max}$) at the minimum bus voltage rating of the converter ($V_{bus\ min}$), as follows:

$$a = \frac{N_P}{N_S} = \frac{V_P}{V_S} \tag{36}$$

Let $D_{max}$ be about 70% and $V_{bus\ min}$ be about 320 V. The transformer turns ratio is calculated as

$$a = \frac{V_P}{V_S} = \frac{(V_{bus\ min} - 2V_M)D_{max}}{V_{load} + V_M} = 4.1 \tag{37}$$

where $V_M$ is the primary Mosfet switch voltage drop and it is assumed to be 0.5 V in calculations.

Let a = 5. The effective operating duty cycle ($D_{eff}$), also called the effective phase shift, is calculated as

$$D_{eff} = \frac{(V_{load} + V_M)a}{(V_{bus} - 2V_M)} = 0.675 \tag{38}$$

2. The transformer magnetizing inductance ($L_m$) is designed based on the maximum magnetizing inductance to realize ZVS as given [33,36]

$$L_m = \frac{T_{dead}\ a\ V_{load\ min}}{C_{HB}\ V_{bus\ min}} * \left(\frac{T_{s\ min}}{4} - \frac{T_{dead}}{2}\right) \tag{39}$$

where $C_{HB}$ denotes the entire equivalent capacitance of the primary H bridge, which can be found on the primary switch datasheet. $T_{s\ min}$ is the minimum switching time, which is determined by the intended minimum switching frequency; $T_{dead}$ is the PWM dead time, which may be computed using the effective duty ratio previously obtained.

3. When selecting the transformer core size, shape, and material, the main considerations are its efficiency, temperature rise, operating frequency, eddy currents, and core losses. For high-frequency applications (10 kHz–3 MHz), iron powder cores, amorphous steel cores, and ferrite cores can be used. However, ferrite cores serve as efficient insulators to prevent eddy currents and experience low core loss. When choosing the core, it is also possible to begin with a core weight ($W_e$), a core effective volume ($V_e$), or a core effective area ($A_e$) based on the transfer power and switching frequency and choose which core will be most appropriate in these terms.

In this work, the ferrite core supplied by TDK [36], with a PQ shape and an effective area of about 200 mm$^2$, is considered excellent for the DC–DC converter switching frequency ($f_{sw}$ = 100 kHz) and high-power density. For acceptable core losses, usually, the transformer magnetic flux should be maintained at a low level (0.1–0.4 Tesla). Therefore, we limit the maximum magnetic flux ($B_{max}$) to 0.35 Tesla, and consequently, the number of primary turns ($N_p$) is calculated as

$$N_P = \frac{V_{bus} \times D_{eff}}{2 \times B_{max} \times A_e \times f_{SW}} = 19.10\ Turns \tag{40}$$

Using an HF transformer with 20 turns of the primary winding, the operating maximum magnetic flux is calculated to be about 0.336 Tesla.

4. Three main losses in the transformer have to be calculated: the core losses, the primary copper losses, and the secondary copper losses.

- For the ferrite cores, the transformer core losses can be calculated as [37]

$$P_{tr\ core\ loss} = 0.036 \cdot \left(\frac{f_{sw}}{10^3}\right)^{1.64} \cdot (10 \cdot B_{max})^{2.68} \cdot V_e \cdot 10^3 \tag{41}$$

- The primary winding RMS current and the copper losses due to the primary winding resistance ($R_p$) can be calculated as

$$I_{p\ rms} = \frac{I_{load}}{2} \times a \tag{42}$$

$$P_{p\ loss} = I_{p\ rms}^2 .R_p \tag{43}$$

- The secondary winding RMS current and the copper losses due to the secondary winding resistance ($R_s$) can be calculated as

$$I_{s\ rms} = \frac{I_{load}}{2} \times \sqrt{2\ D_{eff}} \tag{44}$$

$$P_{s\ loss} = 2 \cdot I_{s\ rms}^2 \cdot R_s \tag{45}$$

3.1.2. Input Capacitor Design

The DC–DC converter's input capacitor is estimated to match the hold-up time ($t_{hold}$) for the minimum input voltage ($V_{bus\ min}$) given to the converter circuit [16,38].

$$C_{in} \geq \frac{2P_{load}\ \ t_{hold}}{\eta\left(V_{bus}^2 - V_{bus\ min}^2\right)} \tag{46}$$

The RMS current and the power losses due to the ESR of the input capacitor of the DC–DC converter stage are calculated as

$$I_{Cin\ rms} = \sqrt{{I_{p\ rms}}^2 - \left(\frac{P_{load}}{V_{bus\ min} \times a}\right)^2} \tag{47}$$

$$P_{Cin\ ESR} = {I_{Cin\ rms}}^2 \cdot ESR_{Cin} \tag{48}$$

3.1.3. Primary Mosfet Selection

To choose optimal Mosfet switches for the high-voltage side of the isolated phase-shift PWM ZVS DC–DC converters implemented for high-power-density applications, the following are some important considerations:

- Low on-state resistance ($R_{dson}$) for low power losses.
- Fast turn-off switching and higher gate plateau voltage.
- Low gate charge $Q_g$ and low capacitance at the output $C_{oss}$ for designs with a wider ZVS range and less deadtime.
- High $dV_{DS}/dt$ and high $dI_F/dt$ to withstand spikes and overshoots.
- Low thermal resistance to decrease thermal power dissipation.
- Body diode with a high reverse recovery rate. The reverse recovery condition occurs when the body diode of a power Mosfet is switched from on-state to off-state while a current is flowing. The drain–source voltage rises rapidly as a result of this.

The RMS current of the primary Mosfet can be calculated as

$$I_{P\ Mos\ rms} = \frac{I_{load}}{2} \cdot \frac{1}{a} \cdot \sqrt{\frac{1}{2}} \tag{49}$$

The primary Mosfet conduction losses at 150 °C is

$$P_{P\ Mos} = {I_{P\ Mos}}^2 \cdot R_{dson} \tag{50}$$

With the design of the converter with ZVS, the turn-on losses and the losses due to the output parasitic capacitance $C_{oss}$ are zero and only the turn-off losses are considered.

$$P_{P\ Mos\ off} = 0.5\ I_{P\ pk}\ V_{bus}\ t_{off}\ f_{sw} \tag{51}$$

In this work, according to the Mosfet design considerations, the voltage, and the current design requirements of the employed power supply, the Mosfet with part number IPW60R070CFD7 from the Infineon company, with a considerably small $R_{dson}$ (about 70 mΩ at 250 °C and 0.13 Ω at 150 °C), low $Q_g$ (about 67 nC), and considerably low $C_{oss}$ (about 53 pF), is used for the full bridge switches on the primary side of the DC–DC converter stage.

3.1.4. Secondary Mosfet Selection

In the high-power density telecom applications, the secondary current stresses in the DC–DC converter are high, causing high conduction losses in the secondary switches. Thus, to have balanced switching and conduction losses, synchronous rectifier switches on the secondary side must have a considerably low $R_{dson}$.

The secondary switch conduction losses can be calculated as

$$P_{SR\ MOS} = {I_{SR\ Mos}}^2 \cdot R_{dson} \tag{52}$$

where $I_{SR\ Mos}$ is equal to the transformer winding secondary current.

The secondary switch switching losses can be calculated using Equation (20), where the voltage stress of the secondary switches can be calculated on the basis of the effective duty cycle and the load voltage.

$$P_{SR\ Mos\ swit} = f_{sw}\left[0.5 \times \frac{V_{load}}{D_{eff}} \times I_{SR\ pk} \times \left(t_r + t_f\right) + 0.5 \times C_{oss} \times \left(\frac{V_{load}}{D_{eff}}\right)^2\right] \tag{53}$$

According to the specifications of the load voltage and load power, the Mosfet with part number IPP110N20N3, with extremely low on-resistance $R_{dson}$, of about 10.70 mΩ, is optimally designed for the synchronous rectification for the AC–DC switched mode power supplies and is selected in the synchronous rectifier switches.

3.1.5. Load Filter Inductor Design

The filter inductance value $L_f$ is designed on the basis of the specified ripple current $\Delta I_{Lf}$ as a percentage of the full load current (15%), as listed in the design specifications in Table 4. Applying KVL at the secondary circuit of the DC–DC converter stage, the value of the filter inductance can be calculated as

$$L_f = \frac{V_{load}\left(1 - D_{eff}\right)}{\Delta I_{Lf} * f_{SW}} \tag{54}$$

The load filter inductor maximum peak current ($I_{Lf\,pk}$) can be calculated as

$$I_{Lf\ pk} = I_{load} + \frac{\Delta I_{Lf}}{2} \tag{55}$$

Using the $LI^2$ method to select the inductor core from the Kool Mu chart as shown in Figure 12, the single-core Kool Mμ with part number 77493 was chosen for the load filter inductor design. The number of turns ($N_{Lf}$) to obtain the required inductance value ($L_f$) can be calculated as

$$N_{Lf} = \sqrt{\frac{L_f}{A_{L\_min}}} \tag{56}$$

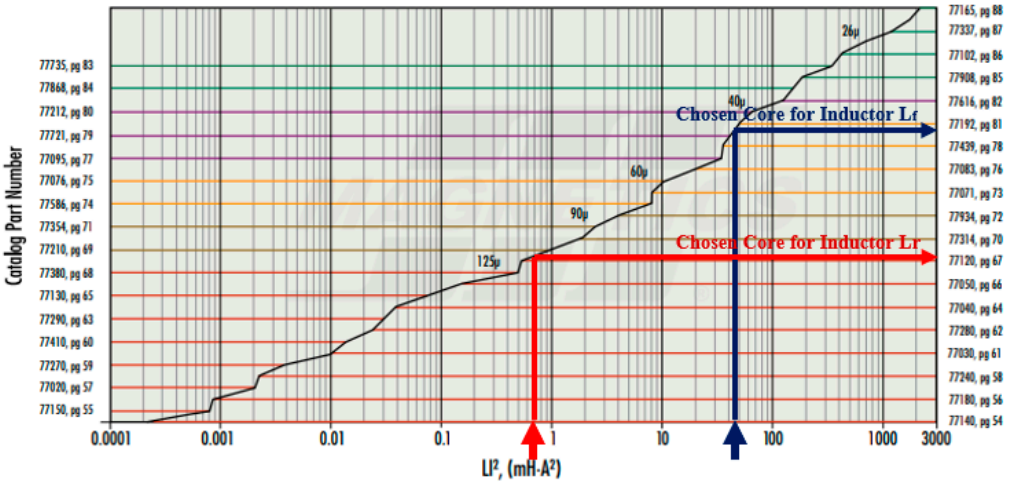



**Figure 12.** Kool Mμ chart for choosing $L_r$ and $L_f$ inductors core for the phase shift PWM converter.

The copper loss ($P_{Lf\,DCR}$) of the winding wire due to the inductor DCR can be calculated on the maximum value of the RMS inductor filter current ($I_{Lf\,RMS}$) given as

$$I_{Lf\ rms} = \sqrt{\left(\frac{P_{load}}{V_{load}}\right)^2 + \left(\frac{\Delta I_{Lf}}{\sqrt{3}}\right)^2} \tag{57}$$

$$P_{Lf\_Loss} = {I_{Lf\ rms}}^2 \times DCR \tag{58}$$

The core losses of the load filter inductor can be calculated using Equation (11), given in calculations of the boost inductor core losses of the PFC stage.

In this work, to design an inductor that can withstand the peak current of about 39.80 A, a load filter inductor ($L_f$) of 30 uF was manufactured with 16 turns of three-wire copper 1.15 mm in diameter around the Kool Mμ 77439A9 toroids core, which also reduces the equivalent DCR value by increasing the wire's cross-section area. The manufactured load filter inductor DCR value was experimentally measured, and it was about 0.0029 Ω.

### 3.1.6. Load Filter Capacitor Selection

The load filter capacitor value ($C_f$) is calculated on the basis of the hold-up time ($t_{hold}$) and the required voltage ripple ($V_{Ripple}$) as follows:

$$C_f \geq \frac{0.9 I_{load} * t_{hold}}{V_{Ripple}} \tag{59}$$

where the hold-up time ($t_{hold}$) is calculated as the time required for the load filter inductor current to reach 90% of the full load current [8].

$$t_{hold} = \frac{L_{load} * 0.9 I_{load}}{V_{load}} \tag{60}$$

The load filter capacitor RMS current is calculated as

$$I_{C_f\ rms} = \frac{\Delta I_{Lf}}{\sqrt{3}} \tag{61}$$

The load filter capacitor value calculated from Equation (59) is about 3300 uF. To reduce the ESR value of the load filter capacitor, 3300 uF capacitance is divided into seven units of electrolytic 470 uF capacitors with *DF* of 0.1 at 63 V, in which the equivalent ESR is decreased by a ratio equal to the number of units. The ESR of the chosen capacitor unit is

about 0.56 Ω, the equivalent resistance ($ESR_{Cf}$) of the output filter capacitor is about 0.08 Ω, and the output filter losses due to the equivalent ESR can be calculated as

$$P_{Cf\ ESR} = {I_{C_f\ rms}}^2 * ESR_{Cf} \tag{62}$$

3.1.7. Resonant Inductor Design

The quantity of energy required to achieve a ZVS condition is used to calculate the size of the resonant inductor tank. As a result, the energy absorbed by the resonant inductance ($L_r$) and transformer leakage inductance ($L_{lk}$) inductor values must be able to exhaust the energy given by the parasitic capacitance of the primary switches ($C_{oss}$) as well as the energy from the transformer winding capacitance ($C_w$).

$$\frac{1}{2} I_{P\ rms}^2 (L_r + L_{lk}) \geq \frac{4}{3} C_{oss} V_{bus}^2 + \frac{1}{2} C_w V_{bus}^2 \tag{63}$$

The leakage inductance of the designed HF transformer is measured on the primary side, and it is about 1.9 uH. The transformer winding capacitor is measured, and it is about 0.90 nF. Using these values, the resonant inductor to realize the ZVS on the primary side can be calculated.

The peak current of the resonant inductor is calculated as

$$I_{Lr\ pk} = \frac{I_{Lf\ pk}}{a} \tag{64}$$

As shown in the chart in Figure 12, the core for the resonant inductor can be selected on the basis of the $LI^2$ value. The resonant inductor number of turns and power losses can be calculated using the procedure given in the design of the load filter inductor.

In this work, the resonant inductor ($L_r$) with a value of 31 uF was manufactured with 22 turns of the single-wire copper 1.15 mm in diameter around the Kool Mμ 77120A7 toroids core. The manufactured load filter inductor DCR value was experimentally measured, and it was about 0.013 Ω.

Table 5 summarizes the electrical specifications of the designed load filter and resonant inductors for the isolated phase-shift PWM ZVS DC–DC converter stage.

**Table 5.** Electrical specifications of the designed resonant and load filter inductors.

| Parameter | Resonant Inductor | Load Filter Inductor |
|---|---|---|
| Actual inductance | 31 uF | 30 uF |
| Peak current | 7.96 A | 39.80 A |
| Core type | Single Kool Mu (77120A7) | Single Kool Mu (77439A9) |
| Inductive factor | 72 ± 8% (nH/T$^2$) | 135 ± 8% (nH/T$^2$) |
| No. of Turns | 22 | 16 |
| Winding wire | Single copper wire 1.15 mm | 3-Wire copper 1.15 mm |
| DC resistance (DCR) | 0.013 Ω | 0.0029 Ω |

*3.2. Power Loss Distribution in the DC–DC Converter Stage*

Table 6 summarizes the design procedure results of the power components and power loss calculations in the employed phase-shift PWM ZVS DC–DC converter stage. The power loss distribution in the stage of different components is also shown in Figure 13. The secondary synchronous rectifier switches are responsible for the highest power losses due to the high current stress. The expected conversion efficiency, calculated from the analysis of the designed phase-shift PWM ZVS DC–DC converter stage, is about 97%.

**Table 6.** Design components and losses of the employed DC-DC converter stage.

| Component | Quantity | Part Number/Description | Power Loss (W) | Efficiency |
|---|---|---|---|---|
| Input capacitance | 1 | EETHC2W471LC | 2.40 | |
| Primary Mosfets | 4 | IPW60R070CFD7 | 12.92 | |
| Resonant inductor | 1 | Core: Kool Mu 77120A7<br>Single wire of 1.15 mm copper<br>22 Turns | 1.815 | 97.00% |
| H.F transformer | 1 | Core: PQ40/40<br>Turns ratio: 20:4:4<br>$L_m$ = 2.8 mH | 7.13 | |
| Secondary Mosfets | 4 | IPP110N20N3 | 19.26 | |
| Filter inductor | 1 | Core: Kool Mu 77439A9<br>3-wire of 1.15 mm copper<br>16 Turns | 15.50 | |
| Filter capacitor | 7 | SamYoung 470 uF 63V | 0.825 | |

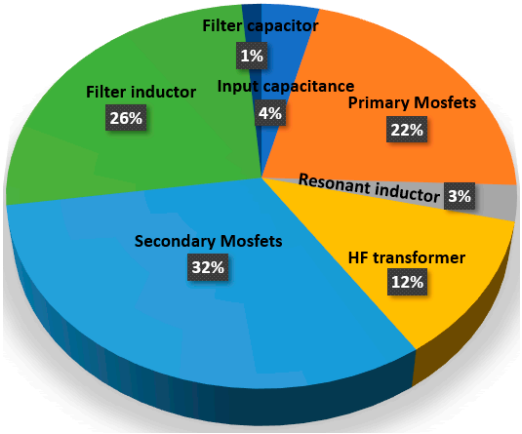



**Figure 13.** Power losses distribution in phase shift PWM ZVS DC-DC converter stage.

### *3.3. Control Circuit Implementation of the Phase-Shift PWM ZVS DC–DC Converter*

By phase shifting the switching pulses of one half-bridge with respect to the other, the phase-shift PWM approach is used to control the full bridge on the primary side of the DC–DC converter. In this part, the ZVS approach is used to provide high-power-density efficient conversion at a high switching frequency. This control section can employ either voltage-mode or current-mode control techniques. Current-mode-controlled DC–DC switching is popular because it is more efficient than voltage mode control. However, when the duty cycle of the PWM rises above 50%, the current-mode architecture can become unstable [38]. The converter primary current slope compensation technique is used to mitigate this instability and restore stability across a large duty-cycle range [39,40].

Figure 14 shows the control strategy of the voltage and current control loops in the DC–DC converter stage implemented in the PSIM software to control the primary and secondary switches of the employed phase-shift PWM DC–DC converter stage.

The feedback signals in this control system are the primary current and the load voltage. To obtain a primary current signal ($V_{Ip}$), a current transformer with a turn ratio of 100:1 is used to sense the primary current, which is then sampled by a resistor. A load voltage signal ($V_{load\_fb}$) is also sensed. To compensate for the instability of current waveforms at high duty cycle values, a 200 kHz ramp signal is added to the $V_{Ip}$ signal to generate the primary current ($I_p$). In the voltage control loop, the load voltage feedback signal ($V_{load\_fb}$) is compared with an appropriate reference value ($V_{ref}$) and passed to the voltage PI controller to generate the primary current reference value ($I_{p\text{-}ref}$). Then, the primary current ($I_p$) is compared with the reference value ($I_{p\text{-}ref}$) to generate the duty cycle required for the phase-shift PWM (PS-PWM) and the synchronous rectifier PWM (SR-PWM)

generators to generate the operating pulse for the primary and secondary switches from $Q_1$ to $Q_6$.

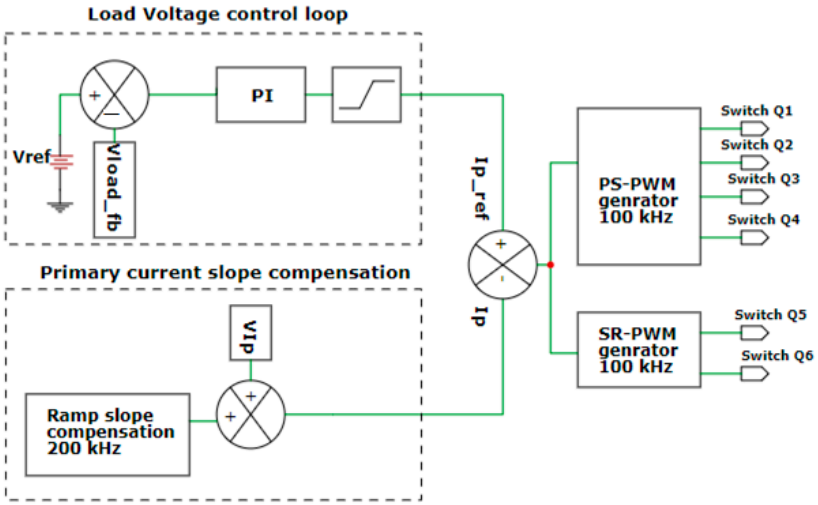



**Figure 14.** Control strategy of the phase shift PWM DC-DC converter stage.

## 4. Simulation Results and Discussions

Figure 15 depicts the overall system structure, as well as the proposed control strategy for the two-stage AC–DC telecom power supply, which was modeled in PSIM software to evaluate the power supply's performance with the optimally designed control loops and the designed power component values (given in Tables 3 and 5) in both the PFC and phase-shift PWM ZVS DC–DC converter stages. As illustrated in the schematic of the PFC stage in Figure 2 as mentioned in Section 2, the EMI filter in the input side of the PFC stage is implemented as a CLC filter with a common-mode (CM) inductor of $L_{cm}$ = 2.2 mH and capacitors of $C_1$, $C_2$, and $C_3$ of 1 uF.

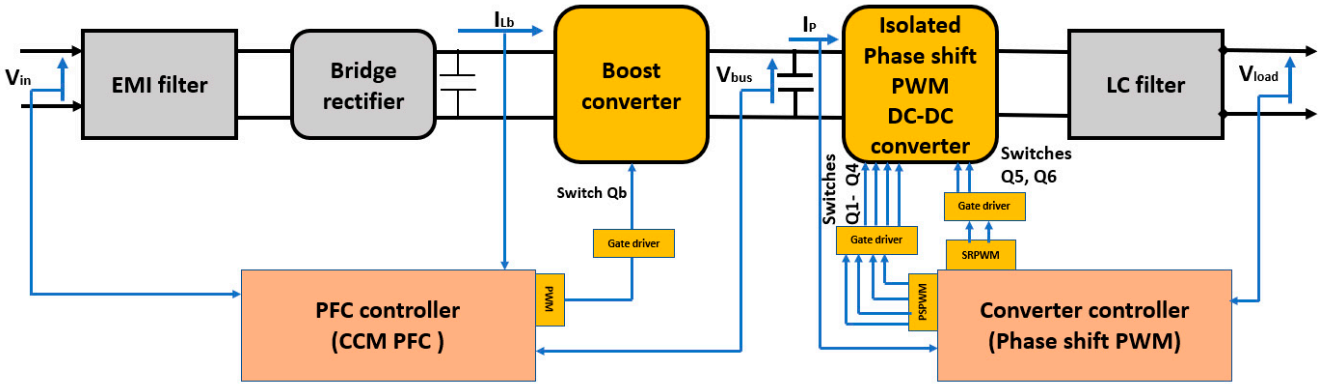



**Figure 15.** Overall system and control strategy of the designed two-stage telecom power supply.

To test the performance of the optimally designed PFC stage current control loop, with a rated supply voltage of 220 Vrms, 60 Hz, and a full loading condition of 2 kW, Figure 16 shows the waveforms of the boost inductor current, the reference current, the supply voltage, and the current, as well as the supply input power factor. The designed control loops succeed in making the inductor current follow the reference current, which reduces the phase difference between the supply voltage current waveforms to less than 5 degrees and offers an input supply with a minimum power factor of about 99.540%.

To test the dynamic performance of the optimally designed PFC stage voltage control loop to regulate the DC bus voltage to the specified value (400 V) with the specified ripple contents (15 $V_{rpp}$) for the wide range of the operating supply voltage, with different supply voltages (minimum voltage = 176 Vrms, nominal range = 220 Vrms, and maximum

voltage = 264 Vrms), the DC bus voltage and the supply voltage are simulated as shown in Figure 17. The figure shows that the designed PFC stage voltage control loop has successfully regulated the DC bus voltage to the specified voltage level with specified ripple limits and with different supply voltages, from 176 to 264 Vrms.

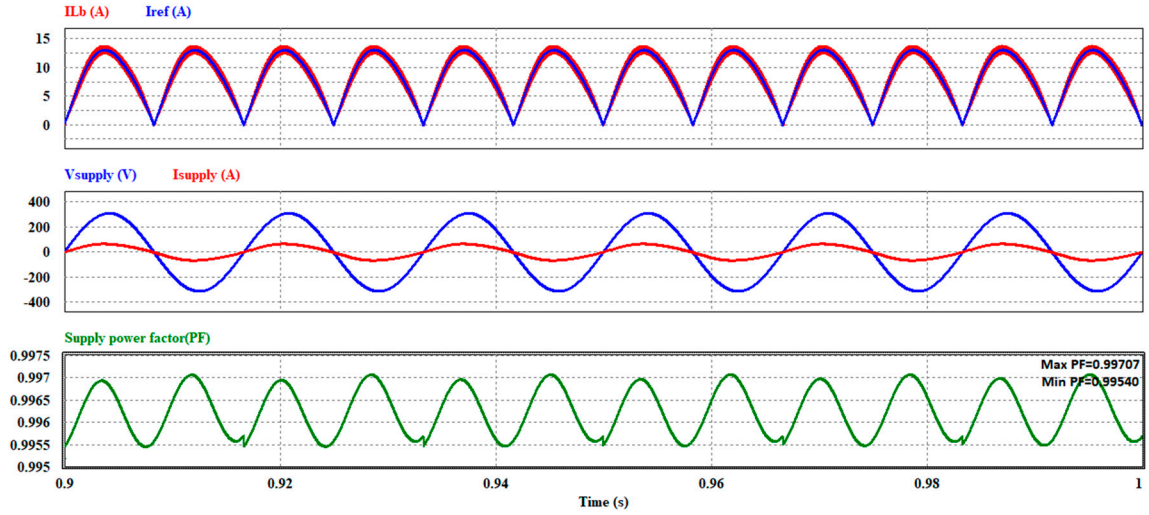



**Figure 16.** Inductor current with reference current, supply current with supply voltage and input PF at 220 Vrms and full loading condition.

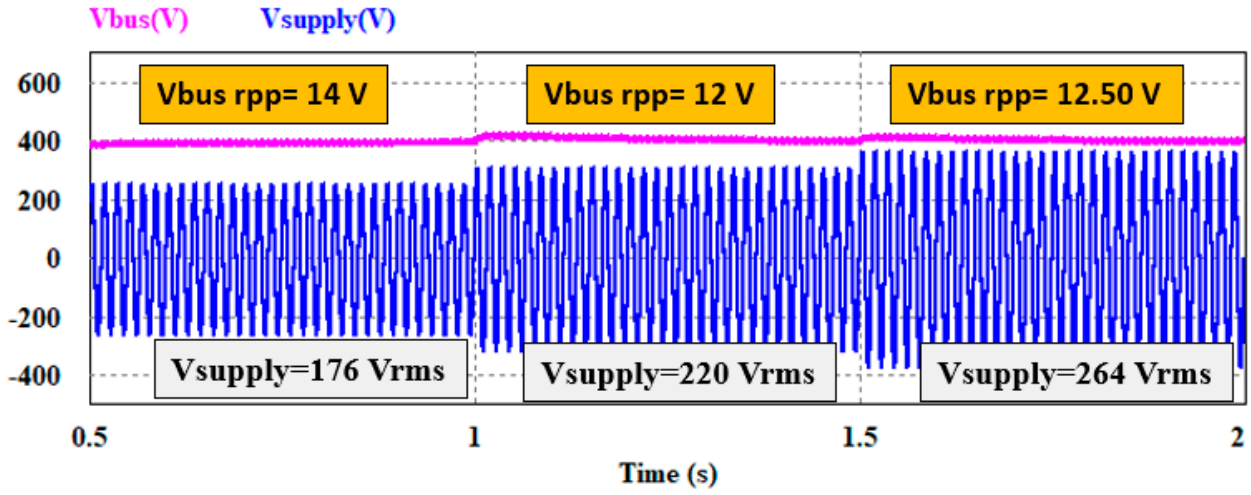



**Figure 17.** DC bus voltage and ripple measurements with different supply voltages.

Figure 18 shows the voltage and current waveforms of the switches $Q_1$ and $Q_3$ in the two legs of the full bridge on the primary side of the phase-shift PWM DC–DC converter stage. For the current waveforms to be clearly observed, they must be multiplied by 20 and show that the designed phase-shift PWM controller and the resonant inductor with the designed value on the primary side of the converter are sufficient to offer switching operation with ZVS in the two legs of the full bridge of the primary side of the DC–DC converter. In addition, Figure 19 shows the ZVS conditions in the voltage and current waveforms of switches Q5 and Q6 in the synchronous rectification circuit of the secondary side of the designed converter.

Figure 20 shows the AC supply, the DC bus, load voltage/current waveforms, and ripple content measurements. With 220 Vrms, and with a full loading condition of 2 kW, the DC bus voltage is regulated to the specified voltage level with a ripple peak-to-peak value of about 12 V, and the designed LC filter on the output load side of the phase-shift PWM converter maintains the load voltage ripple at about 13.5 mV and the load current

ripple at about 20 mA, which is lower than the specified ripple contents for the load voltage and currents.

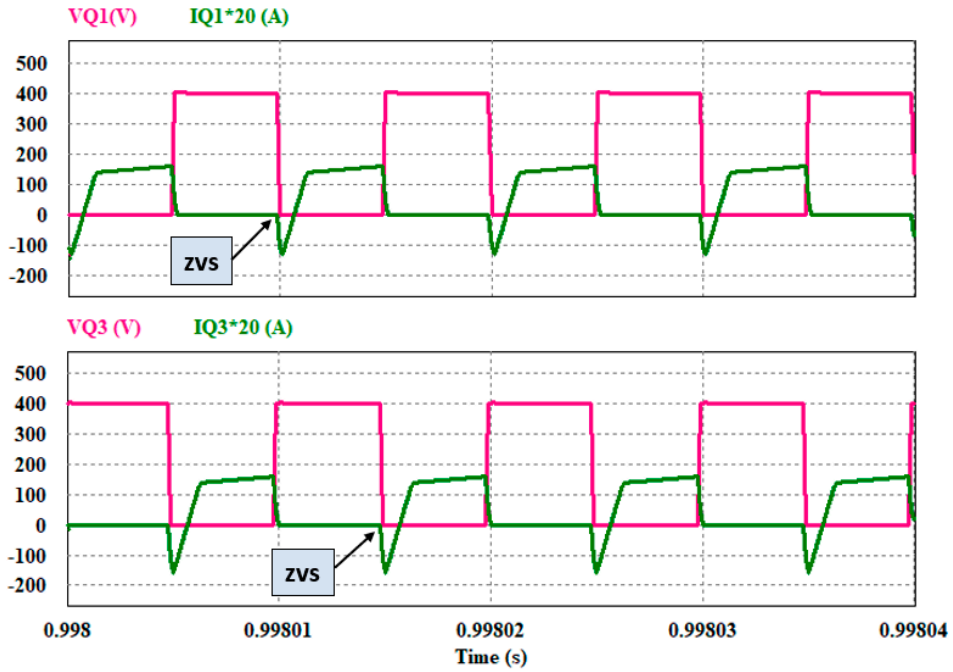



**Figure 18.** Voltage, current waveforms of the primary switches in phase shift PWM converter.

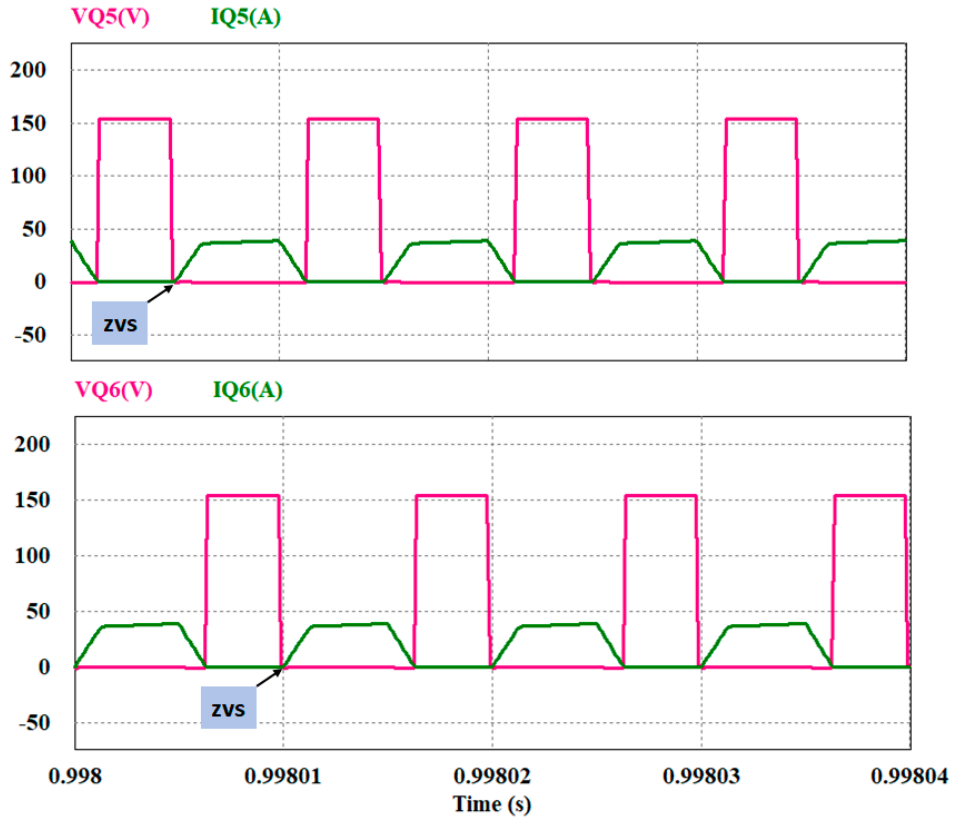



**Figure 19.** Voltage, current waveforms of the secondary switches in phase shift PWM converter.

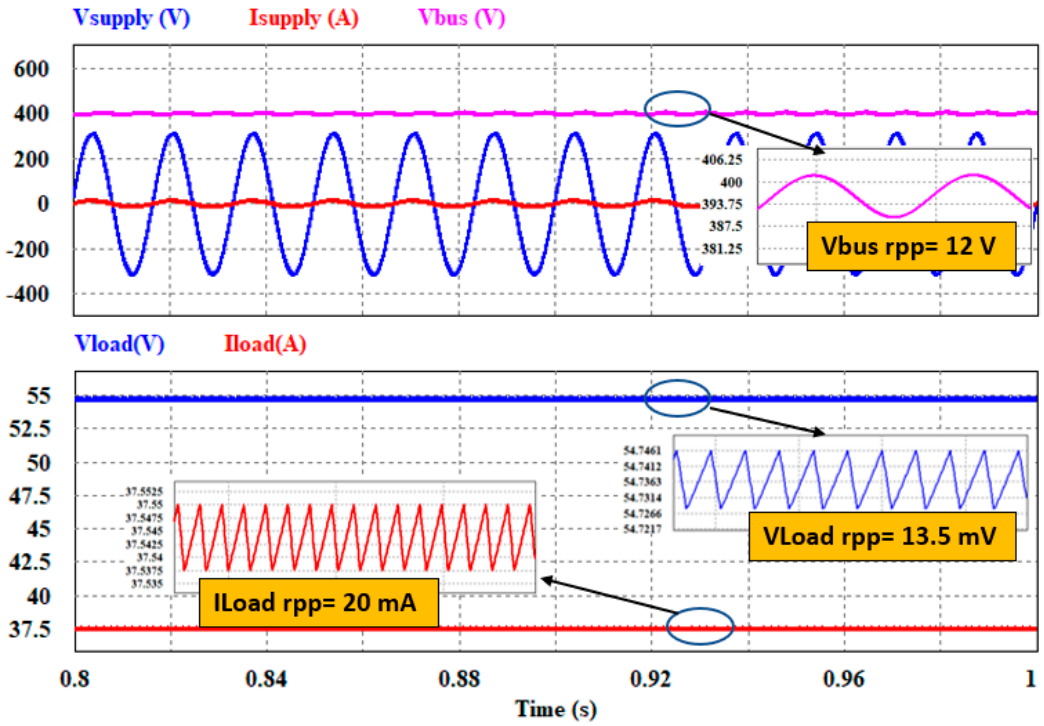



**Figure 20.** Supply, DC bus and load voltage current waveforms with full loading condition.

To demonstrate the total harmonic distortion (THD) in the supply input current, with 220 Vrms and full loading conditions, a fast Fourier transform (FFT) analysis of the supply input current is performed as shown in Figure 21. The analysis shows that the supply current fundamental component of about 13.10 A at 60 Hz and the third harmonic current of about 0.578 A at 180 Hz appear in the frequency spectrum and the total harmonic distortion (THD) measured is about 4.52% for the supply current waveform of the designed AC–DC telecom power supply.

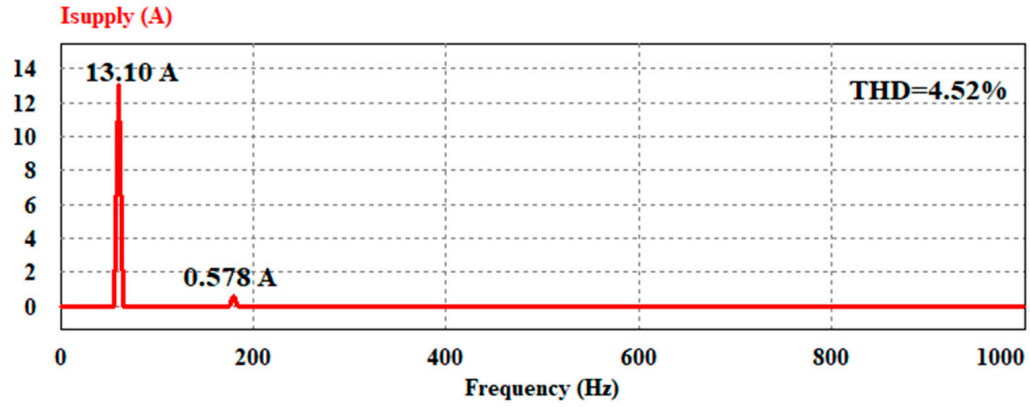



**Figure 21.** Frequency spectrum of the supply current with 220 Vrms and full loading condition.

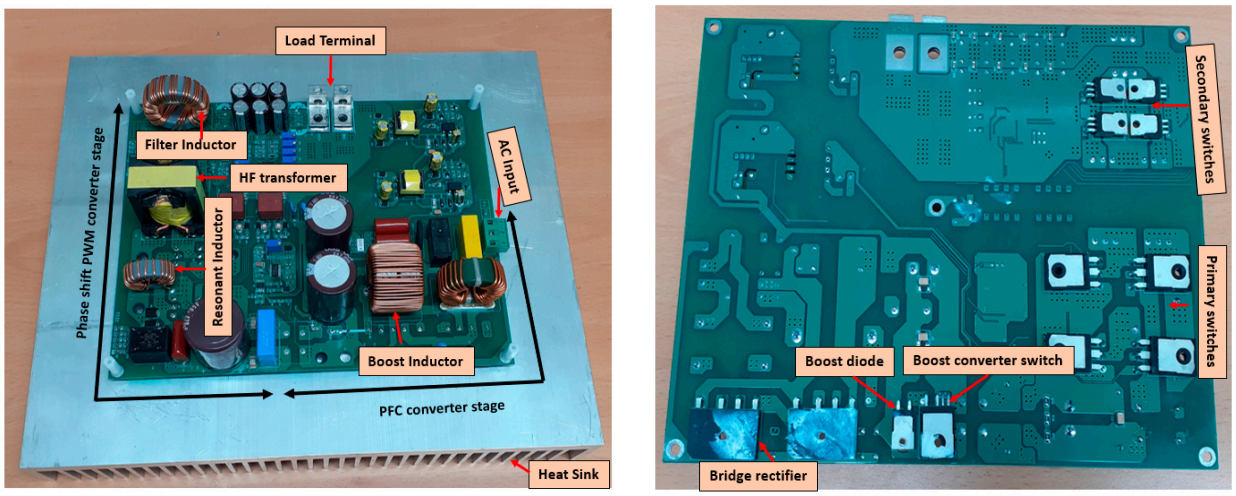
The power loss budget of the different power components was estimated using the PSIM simulation model of the designed two-stage power supply at a full loading condition of 2000 W, as given in Table 7. The efficiency of both stages, as well as the overall efficiency of the designed two-stage power supply, were calculated, where the designed power supply offers an overall efficiency of around 94.50%, and the total full load power losses are around 111.50 W. The PFC stage has a power loss of approximately 6.50 W with a 97.20% efficiency, whereas the DC–DC converter stage has a power loss of approximately 55 W with a 97.25% efficiency.

**Table 7.** Power losses estimation with using PSIM software.

| Component | Power Loss (W) |
|---|---|
| Bridge rectifier | 20.10 |
| Boost inductor $L_b$ | 17.25 |
| Mosfet $Q_b$ | 6.10 |
| Diode $D_b$ | 9.00 |
| DC bus capacitor $C_b$ | 3.90 |
| Input capacitance | 2.40 |
| Primary Mosfets | 11.45 |
| Resonant inductor | 1.65 |
| H.F transformer | 6.45 |
| Secondary Mosfets | 17.65 |
| Filter inductor | 14.35 |
| Filter capacitor | 0.825 |

## 5. Experimental Verification and Discussions

As shown in Figure 22, the printed circuit board (PCB) for the two-stage 2 kW AC–DC power supply for the outdoor telecom power servers is designed and fabricated using OrCAD capture and PCB design software 17.4 (Cadence, Rochester, USA) using the optimally designed and manufactured components of the PFC and the phase-shift PWM DC–DC converter given in Tables 3 and 5.




(**a**) (**b**)

**Figure 22.** Printed circuit board (PCB) of the designed power supply (**a**) Top side; (**b**) Bottom side.

The UCC28180 CCM PFC controller is used to control the PFC stage, which has a switching frequency of about 100 kHz. The UCC28950 IC from Texas Instruments also provides 4-PSPWM signals with a switching frequency of 100 kHz for the switches on the primary side and 2-SRPWM for synchronous rectification at the switches on the secondary side, as well as primary current compensation to restore current stability and voltage loop control to adjust the output voltage to the specified value to control the DC–DC converter switches. Using the design tools of the IC UCC28180 in the PFC stage, the biasing resistor and capacitor values of the controller's pins can be scaled on the basis of the same optimal design specifications of the voltage and current control loops derived based on the small-signal modeling and optimal stability criteria and used in the simulation section.

Figure 23 shows the photograph of the experimental setup used for testing the fabricated power supply. The 3 kW DC electronic load from KIKUSI is connected to the load terminals to test the loading condition of the designed power supply. The voltage-current of the supply, the DC bus, and load terminals, as well as the THD, the PF, and the conversion

efficiency of the designed power supply, are tested under different loading conditions and compared with the results obtained from the simulation process.

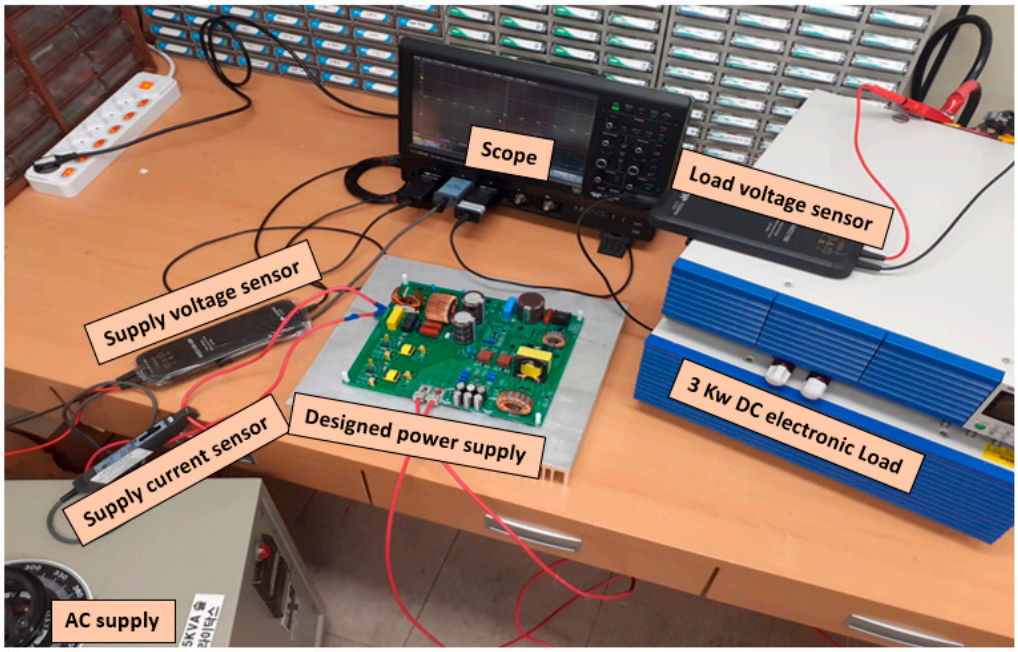
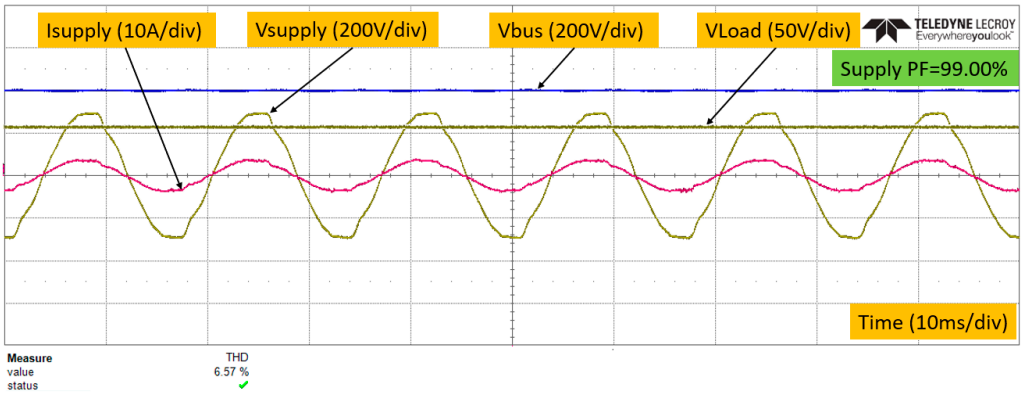


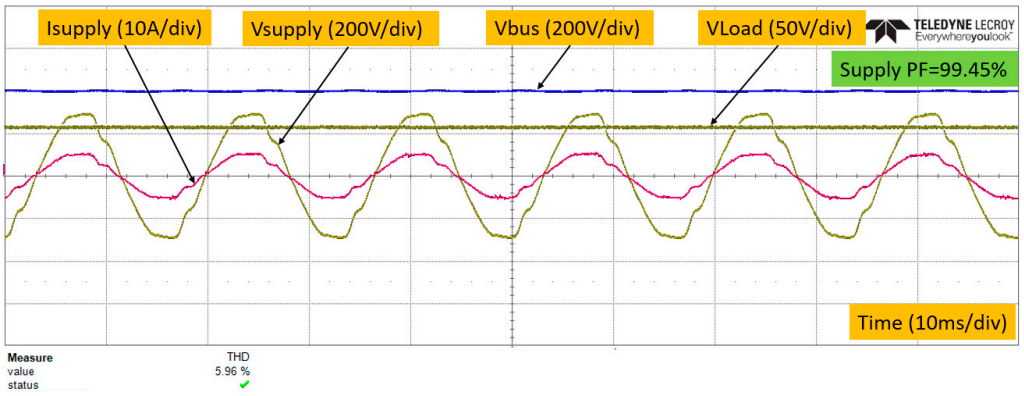

**Figure 23.** Photograph of the experimental setup.

With the light loading conditions of 500 W and 750 W, the experimental performance of the designed AC–DC power supply is investigated as given in Figure 24. As shown in Figure 24a, with a 500 W loading condition, the designed PFC stage current control loop offers an input current with a PF of about 99.00% and a THD level of about 6.57%. The designed voltage control loop in the PFC stage regulates the DC bus voltage to the specified value of about 400 V, and the voltage control loop with the inserted designed LC filter in the load side of the DC–DC converter stage regulates the load voltage at about 54.5 V with a ripple voltage of less than 35 mV. As shown in Figure 24b, when the load power increased to about 750 W, the DC bus and the load voltages were still at constant values, the PF of the designed power supply increased to about 99.45%, and the THD value was about 5.96%.




(**a**)

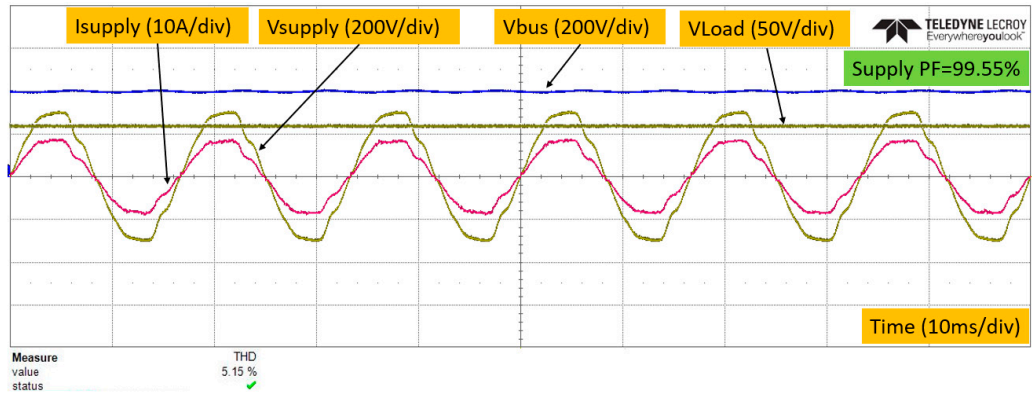
**Figure 24.** *Cont.*



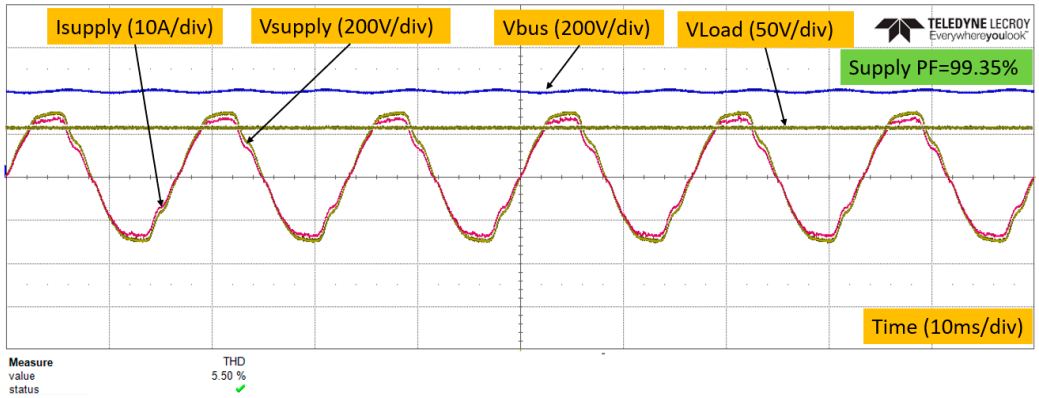

(**b**)

**Figure 24.** Experimental waveforms of the supply voltage-current, DC bus voltage and load voltage as well as the supply PF and THD measurements with 220 Vrms and light loading conditions: (**a**) 500 W; (**b**) 750 W.

The performance of the designed AC–DC power supply is also investigated with high loading conditions of 1250 W and 2000 W, as shown in Figure 25. The designed power supply offers an input PF of about 99.55% with a THD of about 5.15% when the loading condition is about 1250 W, as shown in Figure 25a. At the full load condition of 2000 W, the input PF is about 99.35% and the THD is about 5.50%, as shown in Figure 25b.




(**a**)




(**b**)

**Figure 25.** Experimental waveforms of the supply voltage-current, DC bus voltage and load voltage as well as the supply PF and THD measurements with 220 Vrms and high loading conditions (**a**) 1250 W; (**b**) 2000 W.

With 220 Vrms and different loading conditions (20%, 40%, 60%, 80%, and 100% of the full loading condition), the input and output power of the designed power supply

is measured using simulation and experiment and the efficiency curve is depicted as shown in Figure 26. The minimum efficiency of the designed power supply is measured experimentally at 20% of the full loading condition, and it is about 92.10%. The maximum efficiency is about 94.10% at 80% of the full loading condition, and the efficiency at the full loading condition is about 93.15%. At the full loading condition, the total losses of the designed power supply were measured with experimental tests of about 137 W, where the PFC stage introduces a power loss of about 63 W and the phase shift PWM DC-DC converter stage introduces a power loss of about 74 W.

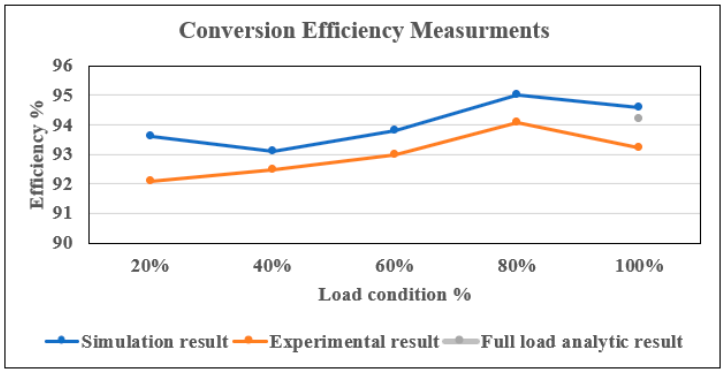
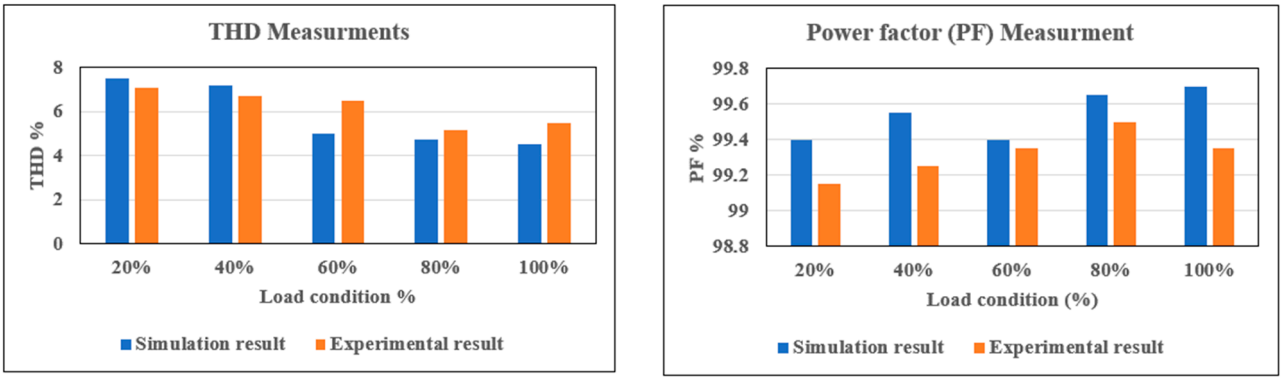



**Figure 26.** Conversion efficiency curve of the designed power supply.

The error in the efficiency from the analytical analysis and from the simulation is calculated as a percentage of an exact experimental efficiency result. The proposed analytical analysis of the two-stage power supply provides efficiency calculation with an error of about 1.10%, and the error in the efficiency calculated from simulation modeling is about 1.72%. These error percentages present the power losses which are not considered in our design in this step, such as the thermal power losses of the magnetic parts, the heat sink, the power losses in the gate drives, and both controllers' Ics.

The supply power factor (PF) and supply current THD values are measured through simulation and experimental tests using 220 Vrms and different loading conditions (20%, 40%, 60%, 80%, and 100% of the full loading condition), as shown in Figure 27. It is observed that the designed power supply THD value measured from simulation and experiment is less than 8% at the 20% to 100% loading condition and about 5.50% at the full loading condition. Furthermore, the supply PF is greater than 99% at 20% to 100% loading conditions and about 99.35% at the full loading condition.




(**a**) (**b**)

**Figure 27.** THD and PF measurements with different loading conditions: (**a**) THD measurements; (**b**) PF measurements.

Table 8 shows the performance comparison between the designed two-stage AC-DC power supply with the commercialized power supply used for the telecom server power

applications; all the cited power supplies worked with a universal input voltage range, and the PF, efficiency, and THD values were measured at full loading condition and rated input voltage range. It is noticed that the proposed design for the two-stage AC-DC telecom power supply offers conversion with a high power density and maintained the PF, efficiency, and THD values at the higher values required for the telecom server applications as compared with the commercialized two stages of AC-DC power supplies.

**Table 8.** Performance of the proposed power supply with the commercialized ones.

| Design Reference | Design Topology | Power (W) | Efficiency (%) | PF (%) | THD (%) |
|---|---|---|---|---|---|
| proposed | Two stage AC-DC Conventional PFC PS-ZVS converter | 2000 | 93.15 | 99.35 | 5.50 |
| [41] | Two stage AC-DC Bridgeless PFC LLC converter | 500 | 93.20 | 98.90 | 7.40 |
| [42] | Two stage AC-DC interleaved PFC LLC converter | 500 | 94.55 | 99.00 | 8 |
| [43] | Two stage AC-DC Conventional PFC LLC converter | 800 | 94.47 | 99.50 | 2 |
| [44] | Two stage AC-DC Totem pole bridgeless PFC Half bridge LLC converter | 1000 | 96.99 | 96.20 | 8.96 |
| [45] | Two stage AC-DC bridgeless PFC LLC converter | 1600 | 94.20 | 98.90 | 4 |

## 6. Conclusions

In this paper, the design procedure, analysis and optimal control strategy of a two-stage isolated 2 kW AC–DC telecom power supply is proposed, where the PFC current and voltage control loops are designed on the basis of an appropriate stability criterion that offers an experimental input supply with a PF of more than 99% and a THD of less than 6.5% for different loading conditions (20% to 100% of the full loading condition). Furthermore, the optimal design analysis, considerations, and manufacturing techniques of the magnetic parts, as well as the selection methodology of the switching elements in both stages, are proposed; they offer a switching operation with the ZVS technique, a reduction in conduction and switching losses in both stages, and offer PFC and isolated phase-shift PWM ZVS converter stages with about 97% efficiency. Moreover, the printed circuit board (PCB) of the designed 2 kW AC–DC telecom power supply is designed and fabricated. An isolated AC–DC industrial power supply with a power density of about 2 kW, a full-load efficiency of about 93.15%, a full-load PF of about 99.35%, and a THD of about 5.5%, suitable for 5G telecom power servers and data centers, is achieved in this work.

In future work, the design of the voltage, current, and power monitoring systems in the design of telecom power supplies will be carried out using a DSP microcontroller unit (MCU) that is designed to manage the operation of PFC and phase shift PWM controllers in both stages, with the shutdown of PWM signals for both stages occurring when unnormal conditions such as overvoltage and overcurrent are presented. In addition, for the establishment of protection systems for thermal and overheating concerns, a fault diagnosis technique based on the reliability and lifetime estimation study of power supply semiconductor parts will be conducted.

**Author Contributions:** Design and application—The literature review and manuscript preparation, as well as the simulations, were carried out by A.H.O. Experimental results and implementation of the prototype were carried by A.H.O. and J.B. Final review of manuscript corrections was carried out by J.B. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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