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A 2.5-GS/s Four-Way-Interleaved Ringamp-Based Pipelined-SAR ADC with Digital Background Calibration in 28-nm CMOS

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Abstract: A 2.5-GS/s 12-bit four-way time-interleaved pipelined-SAR ADC is presented in 28-nm CMOS. A bias-enhanced ring amplifier is utilized as the residue amplifier to achieve high bandwidth and excellent power efficiency compared with a traditional operational amplifier. A high linearity front-end is proposed to alleviate the non-linearity of the diode for ESD protection in the input PAD. The embedded input buffer can suppress the kickback noise at high input frequencies. A blind background calibration based on digital-mixing is used to correct the mismatches between channels. Additionally, an optional neural network calibration is also provided. The prototype ADC achieves a low-frequency SNDR/SFDR of 51.0/68.0 dB, translating a competitive FoM_W of 0.48 pJ/conv.-step at 250 MHz input running at 2.5 GS/s.

Keywords: analog-to-digital converter (ADC); ring amplifier; time-interleaved ADC; digital background calibration

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1. Introduction

High-speed ADC (fs $\geq$ 1 GHz) plays an essential role in broadband communication systems, such as high-speed digital oscilloscopes, base-station, direct RF receivers, and software-defined radio [1–24]. To achieve a GS/s sampling rate, middle-resolution, and excellent power efficiency, time-interleaved ADC (TI-ADC) is considered to be the optimal architecture choice. Figure 1 shows the conceptual block diagram of TI-ADC, with a full-rate demultiplexer switch in the font-end, an associated multiplexer switch in the back-end, and low-speed channel ADC. Generally, an M-channel ADC would speed up the sampling rate M times. However, the mismatches between channel ADCs would deteriorate the performance of the TI-ADC, especially when the input frequency increases. These mismatches include offset, gain, bandwidth, and timing errors. Compared with the other three mismatches, the timing error (or timing mismatch) is dynamic. As a result, it is difficult to calibrate the timing mismatch since the dynamic timing mismatch error is proportional to the frequency, amplitude, and slope of the input signal.

To overcome the above-mentioned mismatches, many calibration methods [1–22] have been proposed in the past decade. The calibration methods can be divided into analog and digital calibration (or mixed), or foreground and background calibration. Digital calibration is more flexible compared with the analog approach. Background calibration is more attractive since it can track supply, temperature, and aging changes without interrupting normal ADC operation. We review a few proposed solutions here. In [10], a reference ADC (slow, yet accurate) for background calibration is proposed to correct the timing mismatch based on the same input signal is sampled and quantified by the

reference ADC and under-calibrated channel ADC. Nevertheless, the additional reference ADC would increase power and area overheads, and restrict the attainable bandwidth in the application. As the reference ADC generally works at a decimated speed to correct all the channel ADCs in sequence, it will cause a varying input impedance for the overall ADC, which will lead to an additional spur in the output spectrum, and deteriorate the overall performance of the TI-ADC. A statistics-based [11] fully digital background method is proposed using the Taylor series approximation for error calibrations. However, the input signal requires meeting wide-sense stationary characteristics. The autocorrelation-based [12] method utilizes the channel ADCs themselves to estimate the timing mismatch between these channels. In [14], the timing mismatch is estimated by digital-mixing (similar to [12]) and corrects the timing error in the analog domain. In recent works, several digital bind calibration methods have been proposed [15,16] without feedback to the analog domain. The reference-ADC-free approach avoids the problem of the mismatched input impedance of each sub-ADC when sampling. Its fully digital method adds no extra clock jitter compared with digital detection and analog correlation, and is the adopted method in this work.

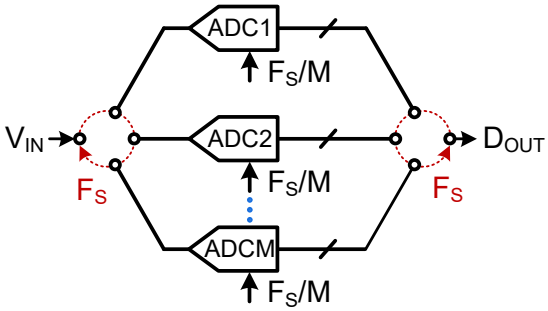

Figure 1. Conceptual block diagram of TI-ADC.

For the channel ADC, a successive approximation register (SAR) is more attractive, due to its outstanding power efficiency [2,4,7,10–12,14–18,25,26]. However, a tremendous number of channels is needed t achieve a high sampling rate. It increases the burden of layout for the clock distribution and assessing crosstalk avoidance since the channel ADC is driven by the divided clock from the clock generator (the long routing and complex interconnects will exacerbate the situation when the number of interleavings increases). However, taking the pipeline architecture as the channel ADC will consume a lot of power to achieve the needed performance, since the power-hungry amplifier is indispensable. In this paper, we explore a pipelined SAR architecture as the channel ADC to achieve a balance between channel number and power consumption. To reduce the power consumption and achieve a nearly rail-to-rail output swing at high input frequency, a bias-enhanced ring amplifier (ringamp) is utilized.

This paper is organized as follows. Section 2 gives a brief review of the ringamp and working principle, mainly focusing on the proposed bias-enhanced ringamp by our previous work. Section 3 discusses the implementation details of the ADC, including the proposed high-linearity font-end, the TI-ADC architecture, routing of the input and clock, the on-chip first-in-first-out (FIFO) memory, and the digital background calibration method. Section 4 presents the measured results of the prototype ADC, and Section 5 concludes this paper.

2. Ring Amplifier Review

With the evolution of the CMOS process, the design of traditional OTA, applied in amplifier-needed ADCs, is facing more and more challenges, such as the decrease of SNR due to the decrease of supply voltage and the decrease of intrinsic gain leading to non-negligible gain errors. Additionally, linearity is an important metric to consider during design [27,28]. A ringamp has been an attractive substitution for OTA, used as a residue amplifier (RA) in pipelined or pipelined-SAR ADCs, since the primary building block

of a ringamp is its inverter [29]. Given its simple inverter-based structure, a ringamp can achieve a large slew-based charge current in large-signal settling phase, low power consumption, and near rail-to-rail output swing. More importantly, ringamps are more suitable for fine CMOS processes and have application scenarios in various types of ADCs due to the versatility of their structures. In the last decade, many ringamp-based ADC works [24,29–39] have appeared. Essentially, there are two different directions of the application, one for high resolution (signal-to-noise-and-distortion-ratio (SNDR) $\geq$ 70 dB) and the other for high speed (sampling rate fs $\geq$ 500 MHz), such as the dual-deadzone RAMP-based two-step SAR ADC [34], which achieves the highest SNDR for a ringamp-based high-resolution ADC, while [33] used a dead zone degeneration technique to realize the fastest sampling rate (fs = 1 GHz) for single-channel implementation.

A ringamp configured in closed-loop feedback typically produces as many poles as the number of inverters, and the dominated pole is located in the output node. Figure 2a shows the topology of a three-stage bias-enhanced ringamp with auto-zero and load capacitors. The self-biased ringamp [30] is replaced by a resistor R_{DZ} inserted in the second stage to separate the signal without additional bias capacitors, enabling the transition of the ringamp from oscillation to amplification, due to the nature of the ringamp, which originates from a ring oscillator. The bias-enhanced ringamp is originally proposed in [31] by inserting a resistor R_{BE} in the first stage and cross-coupling the top and bottom nodes of the resistors to the second stage. Due to the increase in the overdrive voltage of the second stage transistors, bias-enhanced ringamp can achieve larger bandwidth. Typically, for high-resolution applications, high-threshold voltage (HVT) transistors are preferred, in the third stage, to achieve high DC gain and operate in the cutoff region at a steady state, thus reducing ADC gain error and enabling calibration-free operation. Nevertheless, for high-speed application, the transistors in the third stage are typically low-threshold voltage (LVT) transistors to achieve high bandwidth and operate in the sub-threshold region at a steady state.

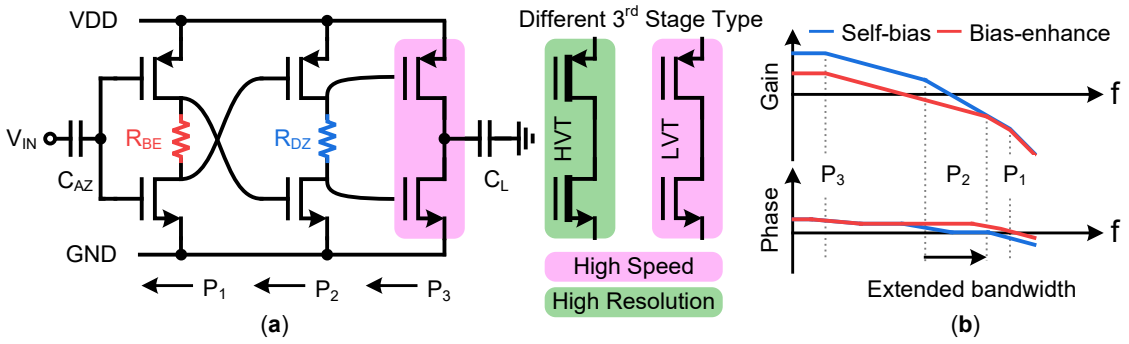

Figure 2. Proposed bias-enhanced ring amplifier for high-speed ADC: (**a**) The schematic of the basic three-stage ringamp and the different configuration in the 3rd stage for various applications; (**b**) The conceptual bode plot to explain the bandwidth extension by the proposed bias-enhanced ringamp.

In this work, we have chosen the LVT transistor as the third stage, to achieve high bandwidth. We have improved the bias-enhanced ringamp with PVT compensation and fast-start circuits based on our previous work in [35]. Figure 2b shows the conceptual bode plot of this self-biased and bias-enhanced ringamp. There are three poles in the ringamp, expressed as

$$P_s = \frac{1}{2\pi R_s C_s} \tag{1}$$

where s stands for the stage number and $s \in \{1, 2, 3\}$, R_s and C_s represent the small-signal resistance and total capacitor, considering the parasitic capacitor in the associated node. Normally, the values of poles meet $P_3 \leq P_2 \leq P_1$. Due to the added resistor, R_{BE}, in the first stage, the overdrive voltages for the second-stage transistors are increased, which leads to an extended bandwidth, assuming the other two poles remain the same, as Figure 2b

shows. Although the loop gain is decreased a little, the bandwidth improvement is more essential for high-speed applications.

3. Proposed ADC Design

3.1. High-Linearity Front-End

The linearity of the high-speed ADC is deteriorated due to the bonding wire and non-linear capacitance of the diode at the input PAD for electro-static discharge (ESD) protection, especially when the input frequency increases. Figure 3a shows the extracted bonding parameters based on the ball grid array (BGA) package followed by the ideal sampling switch and capacitor. The number of ESD diodes is M for the simulations. The simulation result, as Figure 3b shows, is presented as the linearity versus the multiplier of the ESD diodes. The linearity decreases as the multiplier increase since the nonlinear diode capacitor is increased. However, the reliability increases with the number of diodes. In essence, it is a trade-off between linearity and stability. In this work, we choose M = 3 in this design to meet the linearity and reliability requirements.

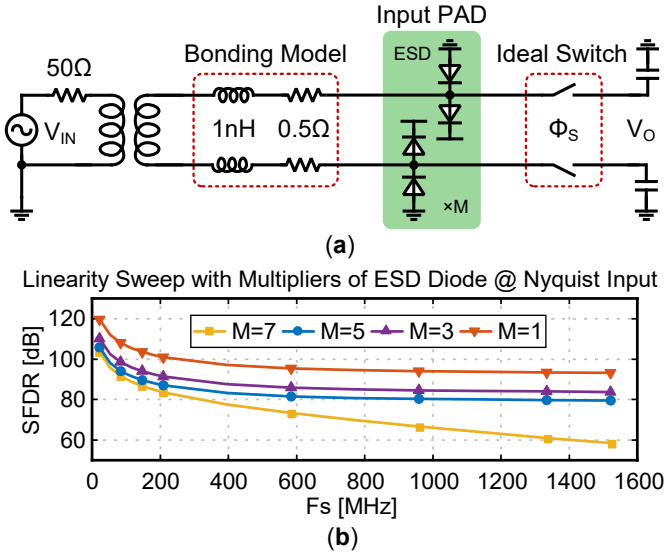

Figure 3. High linearity modified input pad and simulated result: (**a**) The simulation setup to evaluate the linearity of the front-end considering the parasitic model of packaging and ESD diodes; (**b**) The simulation results of linearity versus multipliers of ESD diodes.

To reduce the kickback noise and provide strong driving ability, an input buffer is required in high-speed ADC. Figure 4 shows the adopted replica capacitor-based source follower, maintaining a relatively constant current flowing the $M_{2P/2N}$, thus providing high linearity. Additionally, to reduce the cross-talk between adjacent channels, the input buffer is embedded in the channel ADC as Section 3.2 shows.

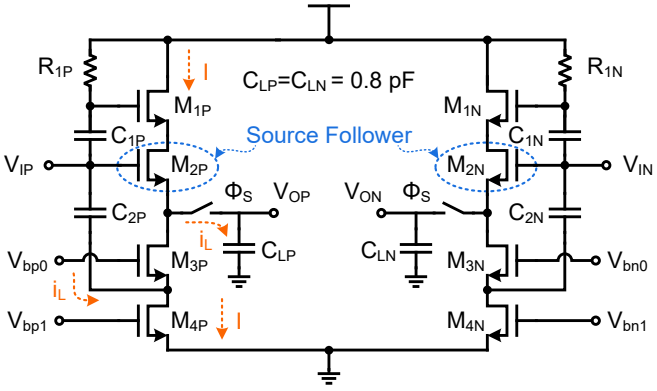

Figure 4. The differential input buffer.

3.2. TI-ADC Architecture

The architecture of SAR-assisted ringamp-based pipelined TI-ADC is illustrated in Figure 5. For the channel ADC, an SHA (sample-and-hold amplifier)-less architecture is adopted. Two MDAC (multiplying digital-to-analog converter) stages are adopted to achieve a high conversion rate, tackling 2.5-bit and 2-bit stages, respectively. For the last stage, which does not require an amplification phase, we use a two-channel time-interleaved asynchronous 9-bit SAR stage to achieve a high conversion rate as well as low power consumption. The 0.5-bit and 1-bit redundancies are adopted in the 1st and 2nd stages, respectively, to alleviate the requirement for comparators. The half-amplification structure used in the 2nd-stage further alleviates the requirement for the 2nd-stage amplifier. More details about the channel ADC can be obtained from [35]. The output data are captured by the on-chip RAM (FIFO, which will be explained in Section 3.3) without decimating the evaluation of the "real" performance of the channel ADC. A statistics-based calibration method is adopted, as in [35], to calibrate the nonlinear gain error of the ringamp for the channel ADC off-chip. After this, the mismatches of the TI-ADC are calibrated in the background, as discussed in Section 3.4 in the off-chip using Matlab.

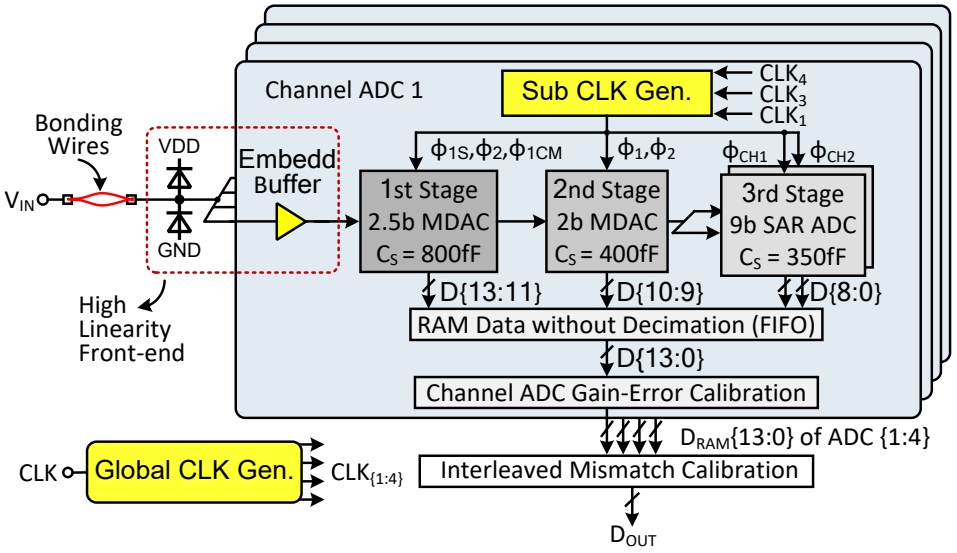

Figure 5. Top-level 2.5 GS/s 12-b four-way TI-ADC architecture (single-ended, actually differential).

The symmetrical differential input and clock routing structure is shown in Figure 6. The differential 2.5-GHz clock signal, $CK_{P/N}$, generated from the clock generator, is divided by four to generate a four-phase 625-MHz clock to drive the four-channel sub-ADC. The differential input, $IN_{P/N}$, is distributed as symmetrically as possible to avoid the even harmonics in the output spectrum. A shield plane is added for the area where the input and clock meet.

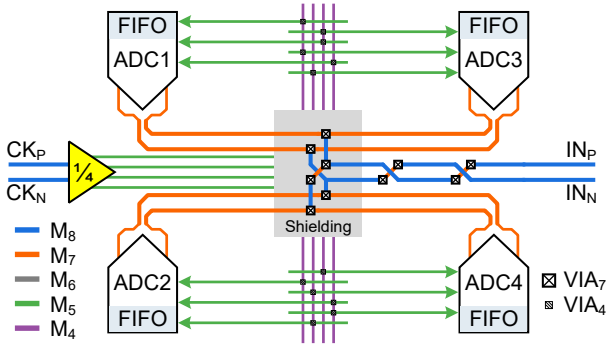

Figure 6. Input and clock routing details.

The timing diagram of the TI-ADC is shown in Figure 7. The TI-ADC is clocked from an external low-noise signal generator, and the four-phase divided clock after the global clock generator is distributed to the channel ADC symmetrically, as Figure 6 shows. The sampling time of the first stage accounts for 25% of the clock period, *TC*, in channel ADC to increase the amplification time of the residue amplifier. For the second stage, the sampling time is 50%, for an easy local clock generator. This two-way interleaved SAR stage achieves the required working speed.

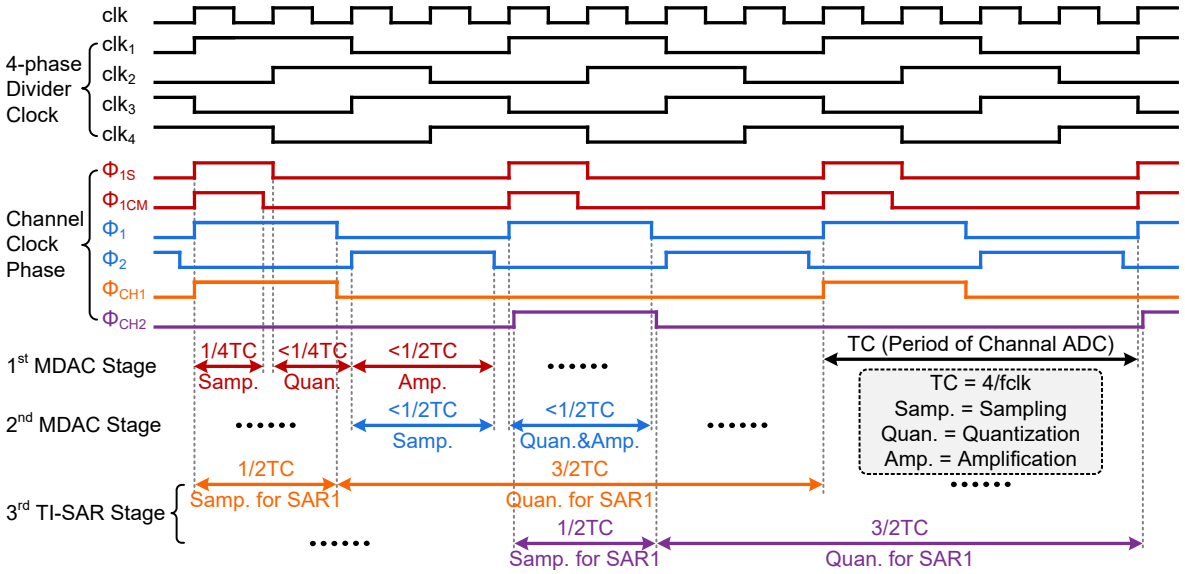

Figure 7. Timing diagram of the TI-ADC.

3.3. FIFO Details

An embedded memory implemented in FIFO with a depth of 8K and a width of 16 bit is adopted is shown in Figure 8a. The FIFO is equipped with an asynchronous clock for *read* and *write*, a reset signal, *RST*, to clear the memory, and the *full* and *empty* signals to indicate the state of the FIFO. When the data is written, the *full* signal is pulled high; then the data is read sequentially, first in, first out, and the *full* signal is pulled low until the data is read. Figure 8b shows the sharing hardware between channel-1,3 and channel-2,4 for PAD saving. The timing diagram for the FIFO is demonstrated in Figure 8c.

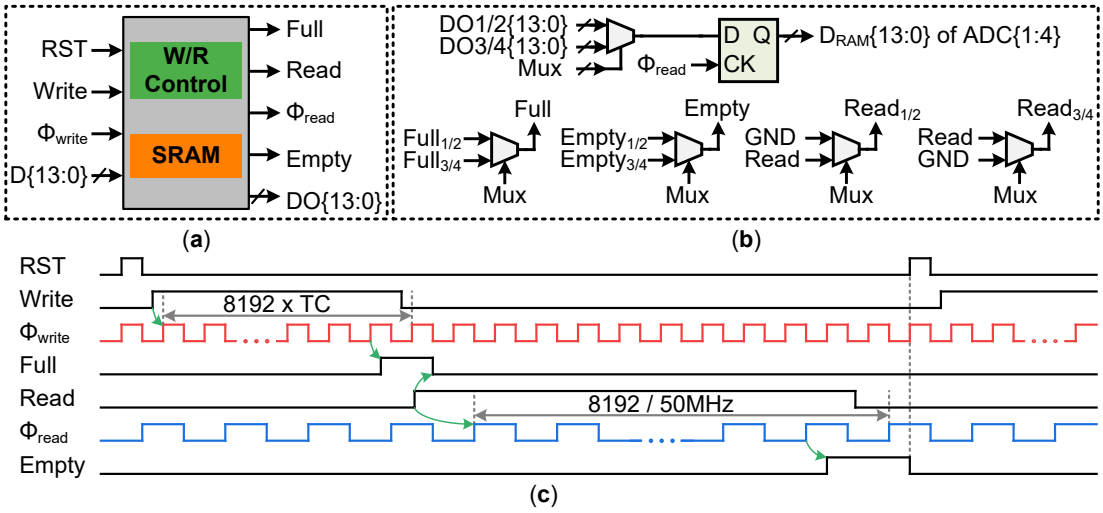

Figure 8. FIFO details: (**a**) Functional block diagram; (**b**) The data selecting and sharing hardware for the adjacent channels; (**c**) The timing diagram for the FIFO.

3.4. Digital Background Calibration

The blind digital background calibration flow is shown in Figure 9a. The offset and gain mismatches can be easily calibrated by averaging and gain normalization. First, each channel ADC removes the offset by subtracting the mean value of the channel code itself. Then, the gain mismatch is calibrated by normalizing the gain factor to the reference channel (ADC1 in this design).

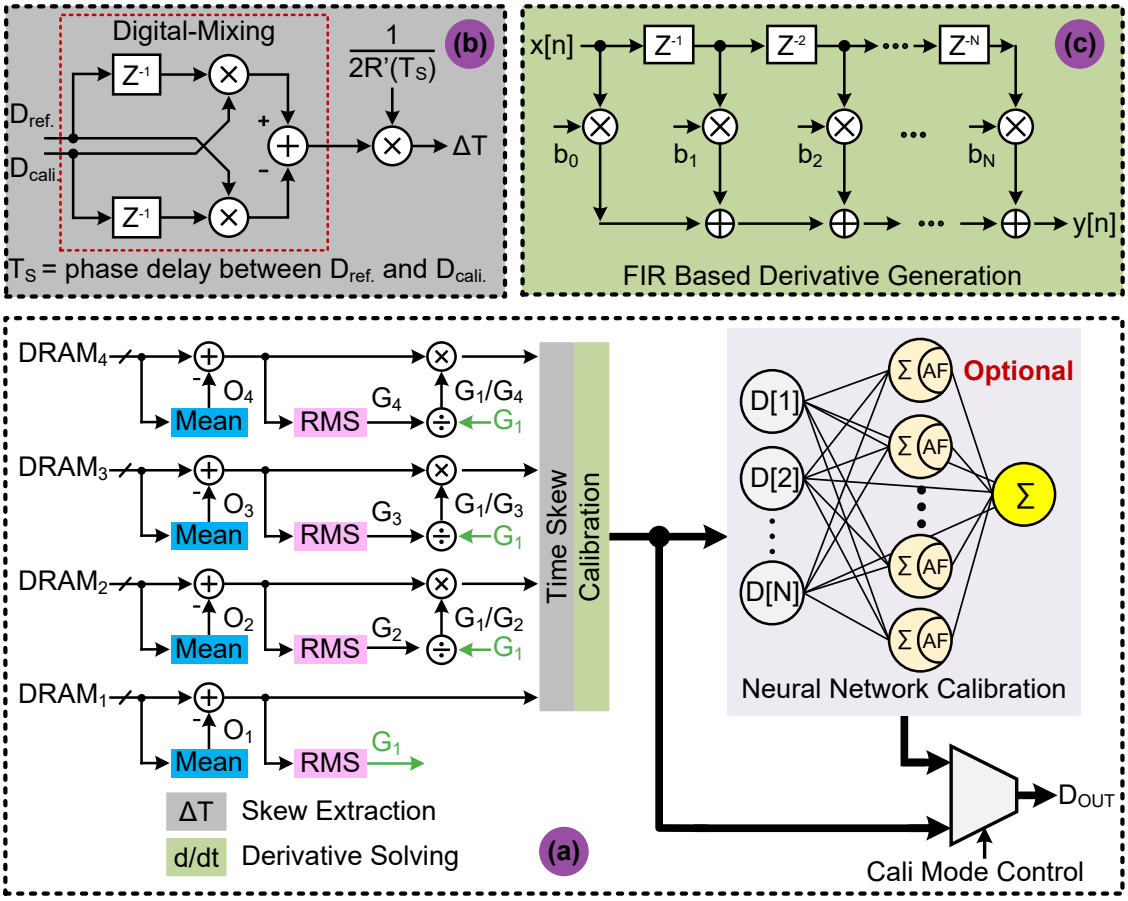

Figure 9. Digital background calibration for offset, gain, and timing mismatch: (**a**) The complete TI mismatches calibration with NNC optional; (**b**) Skew extraction based on digital-mixing; (**c**) Derivative solving based on FIR filter.

The timing mismatch is calibrated using digital mixing [16]. Based on the autocorrelation function, the timing skew ΔT can be calculated as

$$\Delta T = \frac{\overline{D_{\Delta T}}}{2\frac{dR_x}{d\tau}\Big|_{\tau=T_{CK}}} \tag{2}$$

where R_x is the autocorrelation function of input, and $\overline{D_{\Delta T}}$ is the output of the digital mixing (as shown in Figure 9b) between the under-calibrated and reference channels. After getting the timing skew, the calibrated output is

$$D_{cal} = D_{uncal} - D'_{uncal} \times \Delta T. \tag{3}$$

The focal point is to obtain the derivative of the input signal. It is realized using an FIR filter, as shown in Figure 9c in Matlab. The timing skew mismatch calibration sequence behaves in a "middle-search" way. First, the channel 1 data is used to calibrate channel 3. Next, the calibrated channels 3 and 1 are used to calibrate channels 2 and 4. Finally, the calibrated 4-channel data are merged to the final output of the TI-ADC. An optional

neural network calibration (NNC) is also included [40]. The measurement results with and without NNC are shown in Section 4.

4. Measurement Results

The prototype 12-bit ADC is designed with the standard 28-nm CMOS technology. The measurement setup for evaluating the ADC performance is shown in Figure 10a. The input signal is generated from a signal source (Agilent E8267D), followed by a band-pass filter with a center frequency equal to the input frequency (not shown in the figure) to guarantee the spectrum purity. The low-phase-noise clock is generated by a signal source (Agilent E8257D). Three separate power supplies for high-voltage input buffer (2.0 and −0.5-V), high-noise digital power (1.0-V), and low-noise analog power (1.0-V) are provided by the low-dropout regulator on the printed circuit board (PCB). The FIFO data are read by an Agilent logic analyzer 16822A with control signals to meet the timing diagram of the FIFO. The captured data are reconstructed and calibrated on a host PC. Figure 10b shows a microphotograph, wherein the core occupies an area of 1936 µm × 896 µm, and the remaining chip area is filled with the decoupling capacitor and pads. The global clock generator is located in the lower center, and the divided output clocks are symmetrically distributed to the channel ADC. The input signal is poured from the upper center pads. To reduce the bonding wire ringing effect, double or triple bonding is adopted in the pad layout and package scheme. Figure 10c shows the "son" board of the PCB and the BGA-196 package chip. To improve the measurement efficiency, a socket for testing is customized, as shown in Figure 10d.

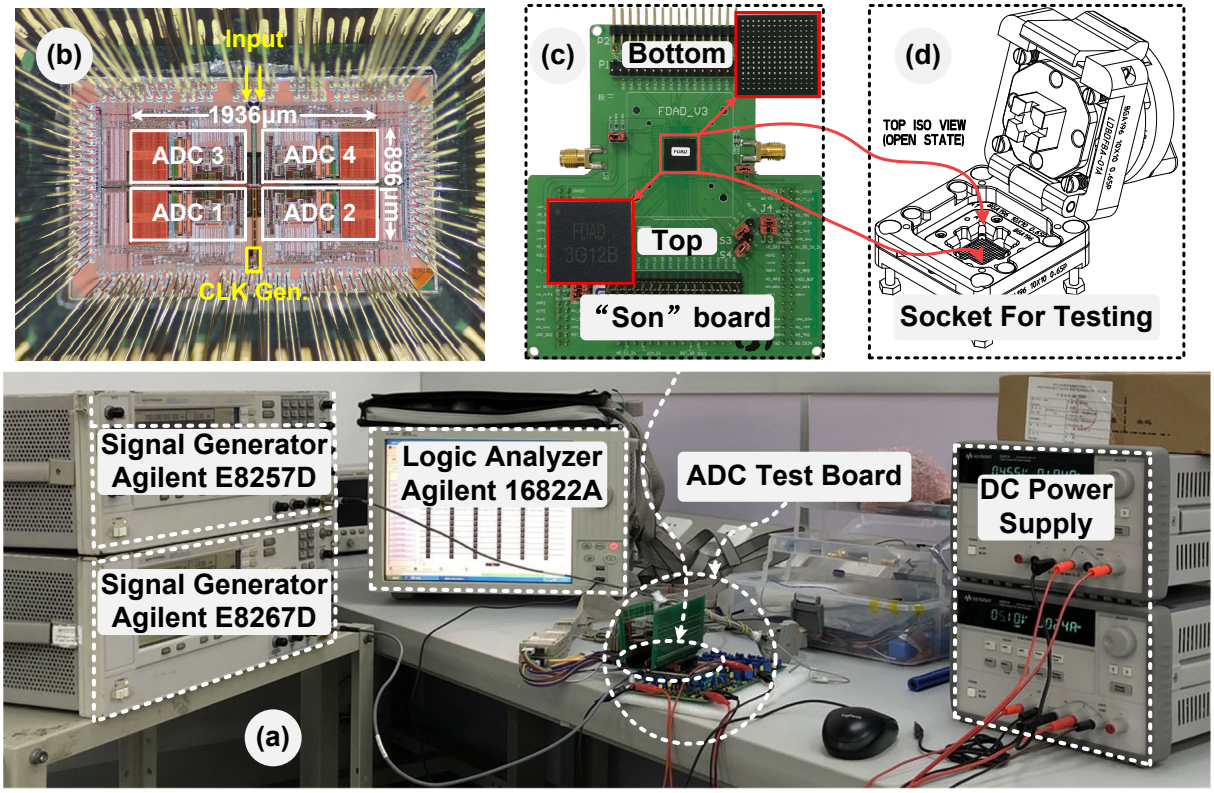

Figure 10. Chip microphotograph and measurement details: (**a**) The measurement setup for the 4-way TI-ADC; (**b**) Chip microphotograph; (**c**) The "son" board and associated BGA package; (**d**) The socket for the BGA testing.

At a 2.5-GS/s working speed under a 1.0-V power supply for the core ADC and 2.0/−0.5-V for the high-linearity input buffer, the total power consumption is 418.4 mW. The core power breakdown is shown in Figure 11. The embedded input buffer in the high-voltage domain accounts for 70% of the total TI-ADC power consumption, where the power of a single buffer is 64.2 mW and the left power is used for the impedance

matching. The residue amplifier accounts for only 30.6% of the core power, which is the main advantage of this ringamp-based pielined-SAR ADC. The measured DNL and INL after calibration are +1.75/−1.00 LSB and +3.31/−2.98 LSB, respectively.

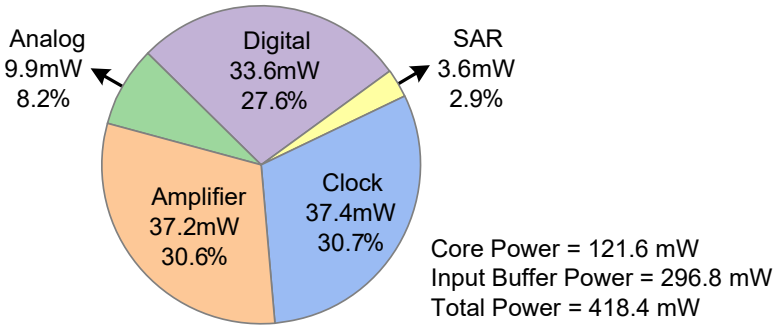

Figure 11. Measured core power breakdown.

The measured FFT spectrum of the proposed TI-ADC with near −1 dBFS input power @ 2.5 GS/s for a 250-MHz input with and without calibration are shown in Figure 12 (NNC is not used). Unless stated otherwise, all measurement results are reported for a sampling rate of 2.5 GHz. After the digital background calibration, the offset, gain, and timing-mismatch spurs are all below −70 dBFS, which will not limit the overall TI-ADC linearity performance. The SNDR improves to 51.0 dB, while the uncalibrated value is only 44.1 dB. The SFDR improves 22 dB without any interleaved spur in the calibrated output spectrum.

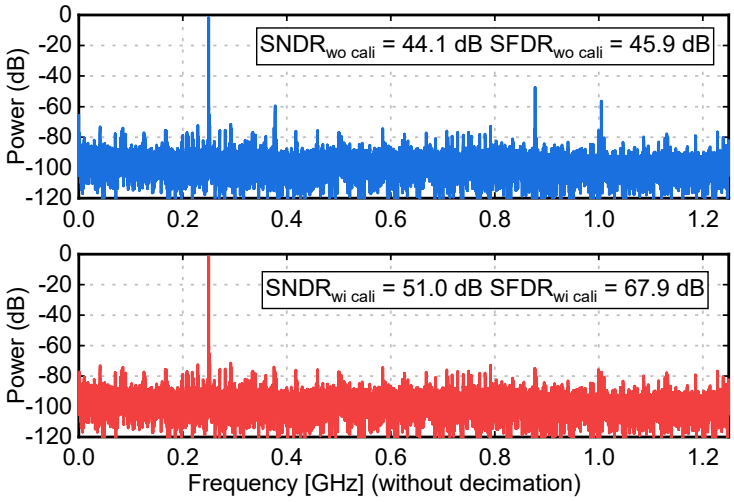

Figure 12. Measured output spectrum for a low-frequency input with and without channel mismatch calibration @ 2.5 GS/s.

The measured FFT spectrum of the proposed TI-ADC @ 2.5 GS/s for a 1-GHz input with digital background calibration and additional NNC are shown in Figure 13. After the digital background calibration, the offset, gain, and timing mismatches spurs are all below −70 dBFS, and the linearity performance is not limited by the interleaved spurs. The performance degradation is mainly due to the large noise (low SNR), especially the clock-jitter noise, which can be verified from the spectrum. The large internal clock jitter is calculated around 650 fs by comparing the low- and high-input frequency SNR performance.

The SFDR improves to 60.1 dB with the NNC turned on, while the value with digital calibration is only 51.7 dB. To summarize, the NNC can improve the linearity performance, however, it does not help the SNR improvement, since the SNR is limited by the circuity-level noise.

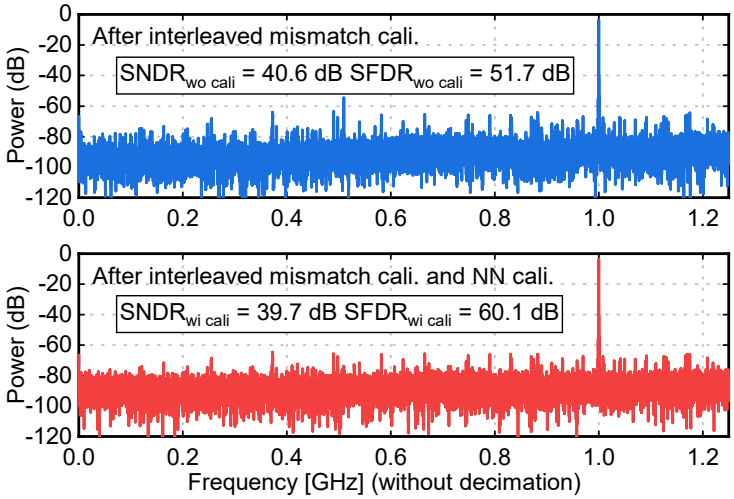

Figure 13. Measured output spectrum for a high-frequency input with and without NNC @ 2.5 GS/s after channel mismatch calibrated.

Figure 14 shows the dynamic performance measured with various input frequencies @ a 2.5 GS/s working rate. Due to the limited power of the signal generator in the laboratory, the input power at 1 GHz is reduced to near −4 dBFS. The results verify the effectiveness of the blind digital background calibration. The deterioration of the performance at high input frequency is mainly caused by the large internal clock jitter around 650 fs and less decoupling of the capacitor for the clock generator to suppress the supply ripple for the clock buffer. The main linearity at high input frequency is caused by the second harmonic due to the imbalance in the test printed circuit board (PCB) routing between the differential input. Additionally, the long routing from the mother-board to the real test "son-board" generated additional noise during ADC measurement. Since the high-output raw data are captured by the on-chip RAM and are read out without any decimation, the output performance will not benefit from the decimation as traditional works have.

Figure 15 shows the dynamic performance measured with various input frequencies @ a 2.0-GS/s working rate. The SFDR improves more than 8 dB for a wide range of input frequencies with the background calibration. Figure 16 shows the dynamic performance measured with various input frequencies @ a 3.0-GS/s working rate. The improvement is less at a high working rate because of the incomplete settling of the ringamp, especially at the high input frequency.

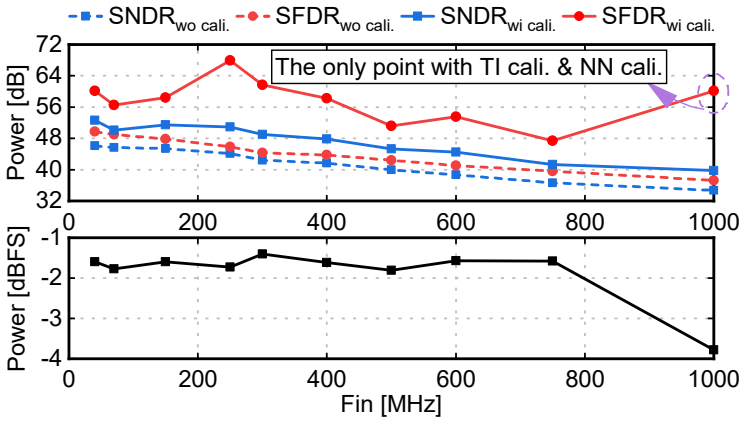

Figure 14. Measured dynamic performance versus input frequency @ 2.5 GS/s and associated input power. (The performance for the 1-GHz input frequency is further calibrated with a NNC, other measurements are based on interleaved mismatches calibration only including Figure 16).

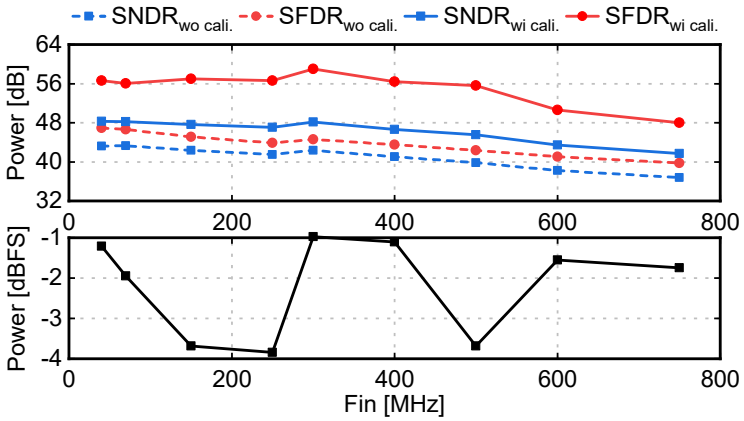

Figure 15. Measured dynamic performance versus input frequency @ 2.0 GS/s and associated input power.

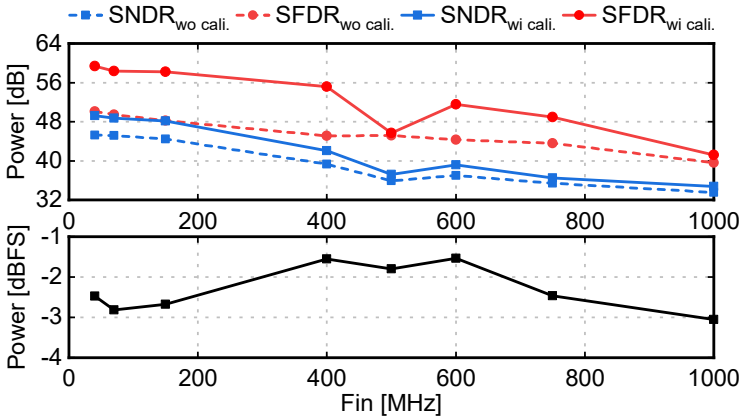

Figure 16. Measured dynamic performance versus input frequency @ 3.0 GS/s and associated input power.

Table 1 summarizes the measured performance compared with the recently published high-speed TI-ADCs. It explors the pipelined-SAR architecture as the channel ADC for the TI-ADC; due to the large power consumption of the input buffer, the total power is not reduced significantly. However, the power of the total ADC is still competitive. The ADC achieves a FoM_w of 0.48 pJ/conv.-step at a 250-MHz input.

Table 1. Performance Summary and Comparison.

Reference	[17]	[18]	[19]	[20]	[21]	This Work
resolution [b]	11	10	12	12	12	12
supplies [V]	1.2/2.5	1.2/1.3/1.6	1.8	2.5	1.8	1.0/2.0/−0.5
architecture	TI-SAR	TI-SAR	TI-Pipeline	TI-Pipeline	TI-Pipeline	TI-Pipelined-SAR
channel number	4 × 16	4 × 16	4	2	4	4
fs [GS/s]	3.6	2.6	2.4	3.0	3.0	2.5
technology [nm]	65	65	40	40	40	28
area [mm^2]	7.4	5.1	9	0.4 [a]	3.9 [a]	1.73 [a]
SNDR [dB]	42.0 [b]	48.5 [b]	49.7 [b]	51.0 [b]	52.3 [b]	51.0 [c]
SFDR [dB]	50.0 [b]	53.8 [b]	60.2 [b]	59.0 [b]	61.5 [b]	68.0 [c]
power [mW]	795	480	420	500	450	418.4 [d]
FoM_w [pJ/conversion-step] [e]	2.15	0.85	0.70	0.58	0.44	0.48 [f]

[a] Core area. [b] Measured @ near-Nyquist input frequency. [c] Measured @ low input frequency. [d] Measured for near-Nyquist input at 1.0 V and room temperature, excluding calibration power. [e] Walden FoM = Power/(2^{ENOB} × Fs). [f] Calculated @ low input frequency.

5. Conclusions

This paper proposed a ringamp-based pipelined-SAR four-channel TI-ADC. To achieve high linearity, a modified input PAD with a decreased number of ESD diodeswas adopted, which maintained adequate protection. The input buffer with replica load was used to reduce the kickback noise at high input frequency and to maintain high linearity. Additionally, a digital-mixing-based blind background calibration method was used to alleviate the detrimental effects of mismatches among the interleaved channels. An optional NNC was also adopted to achieve high linearity at the high-input frequency. Measured at 2.5 GS/s, the ADC achieved a low-frequency SNDR/SFDR of 51.0/68.0 dB, translating to a competitive FoM_w of 0.48 pJ/conv.-step at 250-MHz input.

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Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary metal oxide silicon
ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
GS/s	Giga samples per second
HVT	High threshold voltage
LVT	Low threshold voltage
ESD	Electro-static discharge
BGA	Ball grid array
SHA	Sample and hold amplifier
RA	Residue amplifier
Ringamp	Ring amplifier
SAR	Successive-approximation register
TI	Time interleaved
NNC	Neural Network Calibration
FFT	Fast Fourier transform
FIR	Finite impulse response
FOM	Figure of merit
LDO	Low dropout regulator
MDAC	Multiplying digital-to-analog converter
SNDR	Signal-to-noise-and-distortion ratio
SFDR	Spurious free dynamic range
FIFO	First input first output
PCB	Printed circuit board

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