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Design of Inner Matching Three-Stage High-Power Doherty Power Amplifier Based on GaN HEMT Model

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Abstract: This paper introduces the structure and characteristics of an internal-matching high-power Doherty power amplifier based on GaN HEMT devices with 0.25 μm process platforms from the Nanjing Electronic Devices Institute. Through parameter extraction and load-pull testing of the model transistor, an EE_HEMT model for the 1.2 mm gate-width GaN HEMT device was established. This model serves as the foundation for designing a high-power three-stage Doherty power amplifier. The amplifier achieved a saturated power gain exceeding 9 dB in continuous wave mode, with a saturated power output of 49.7 dBm. The drain efficiency was greater than 65% at 2.6 GHz. At 9 dB power back-off point, corresponding to an output power of 40.5 dBm, the drain efficiency remained above 55%. The performance of the amplifier remains consistent within the 2.55–2.62 GHz frequency range. The measured power, efficiency, and gain of the designed Doherty power amplifier align closely with the simulation results based on the EE_HEMT model, validating the accuracy of the established model. Furthermore, the in-band matching design reduces the size and weight of the amplifier. The amplifier maintains normal operation even after high and low-temperature testing, demonstrating its reliability. In conjunction with DPD (digital pre-distortion) for the modulated signal test, the amplifier exhibits extremely high linearity (ACLR < −50.93 dBc). This Doherty power amplifier holds potential applications in modern wireless communication scenarios.

Keywords: GaN HEMT; EE_HEMT model; Doherty PA

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1. Introduction

Fifth-generation communication technology (5G) adopts sophisticated modulation techniques such as QAM (quadrature amplitude modulation) and OFDM (orthogonal frequency division multiplexing), resulting in a high peak-to-average power ratio (PAPR) in its signal waveform [1,2]. Doherty power amplifiers can maintain high efficiency both in saturation and power back-off, making them suitable for handling 5G communication signals [3]. The schematic diagram of the traditional Doherty architecture is shown in Figure 1. The quarter-wavelength line after the auxiliary amplifier achieves load modulation performance through impedance transformation. The introduction of a 90-degree phase difference at the input ensures phase alignment between the two amplifiers. However, this architecture can only achieve a power back-off range of about 6 dB, which falls short of meeting the requirements for processing signals with high PAPR.

Asymmetric architectures, as illustrated in the literature [4–14], have improved the traditional Doherty power amplifier structure to enhance its power back-off range. The auxiliary amplifier, compared with the main amplifier, has a higher saturated output power, achieving a power back-off range of approximately 7–8 dB. Additionally, two three-stage Doherty structures, as shown in Figure 2a,b, can achieve power back-off ranges greater than 8 dB. The three-stage Doherty architecture in Figure 2a is an extension of the traditional Doherty structure. The carrier amplifier and the first peak amplifier together form a two-stage Doherty power amplifier, which then combines with the second peak amplifier to form a new Doherty power amplifier.

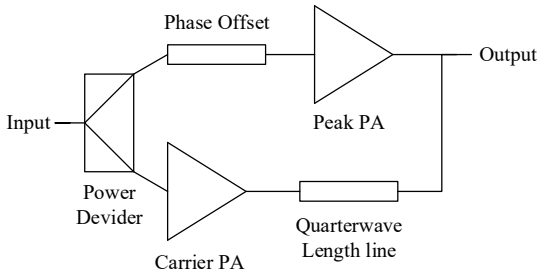


Figure 1. Schematic diagram of traditional Doherty amplifier structure.

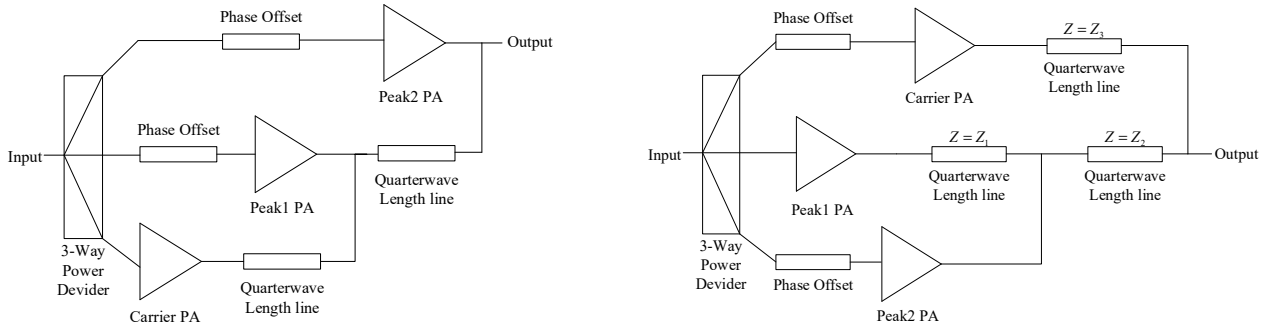


Figure 2. Schematic diagrams of two three-stage Doherty power amplifier structures, (**a**) is extension of the traditional Doherty structure and (**b**) is an improved structure proposed by NXP.

In 2011, NXP proposed an improved three-stage Doherty power amplifier structure [15], as shown in Figure 2b, which has been widely adopted, as documented in references [16–20]. Compared with the architecture shown in Figure 2a, this design effectively improves the gain compression of the main amplifier and further extends the power back-off range. The load modulation behavior of this architecture is analyzed later.

On the other hand, GaN HEMT (gallium nitride high-electron-mobility transistor) devices, due to their broad frequency response and high power density, are widely used in communication, radar, aerospace, and other fields [21–25]. The accuracy of HEMT device models is crucial for MMIC (microwave monolithic integrated circuit) design success and performance. The EE_HEMT model proposed by Agilent Technologies in 1993 is a widely used nonlinear compact model for HEMT devices, providing accurate characterization of the RF properties of the device. Additionally, the EE_HEMT model is a compact model that maintains high accuracy even in scaled applications. In this paper, an EE_HEMT scalable model for a GaN HEMT device with small gate width was established through DC scanning testing, S-parameter testing, and extraction of intrinsic and parasitic parameters. The model was further validated through load-pull testing and simulation, confirming its accuracy in large-signal conditions. The results of testing on the actual circuit indicated close agreement between simulation and measurement, with simulation errors of less than 5% for drain efficiency and less than 1 dB for gain under large-signal excitation, validating the precision of the established EE_HEMT model.

2. Materials and Methods

2.1. Introduction of GaN HEMT Devices

This design utilizes a 7.2 mm gate-width GaN HEMT device developed by Nanjing Electronic Devices Institute. Under a bias condition with a drain–source voltage (V_{DS}) of 28 V, the device can provide a continuous wave saturated output power density exceeding 4.5 W/mm [26]. Its longitudinal structure, as shown in Figure 3a, includes a SiC substrate, an undoped GaN buffer layer, an AlN insertion layer, and an AlGaN barrier layer. The SiC substrate serves the purposes of support, heat dissipation, and electromagnetic shielding. The AlN insertion layer enhances electron mobility to improve high-frequency

characteristics and concurrently reduces scattering effects caused by lattice mismatch. The addition of a gate field plate helps lower the peak electric field, thereby increasing the breakdown voltage of the device. Simultaneously, to minimize thermal resistance and enhance reliability, the SiC substrate is thinned and gold-plated on the reverse, improving heat dissipation capabilities. In addition, the SiN passivation layer covering the entire device surface can effectively enhance the transistor's radiation resistance capability [27]. The entire chip is grounded through vias to minimize parasitic capacitance and inductance, thereby enhancing the high-frequency characteristics of the device. Figure 3b shows a photograph of the GaN HEMT used in this design. The device has a single-finger gate width of 200 μm and a total gate width of 7.2 mm. The overall size of the entire chip is 2.62 mm × 0.93 mm.

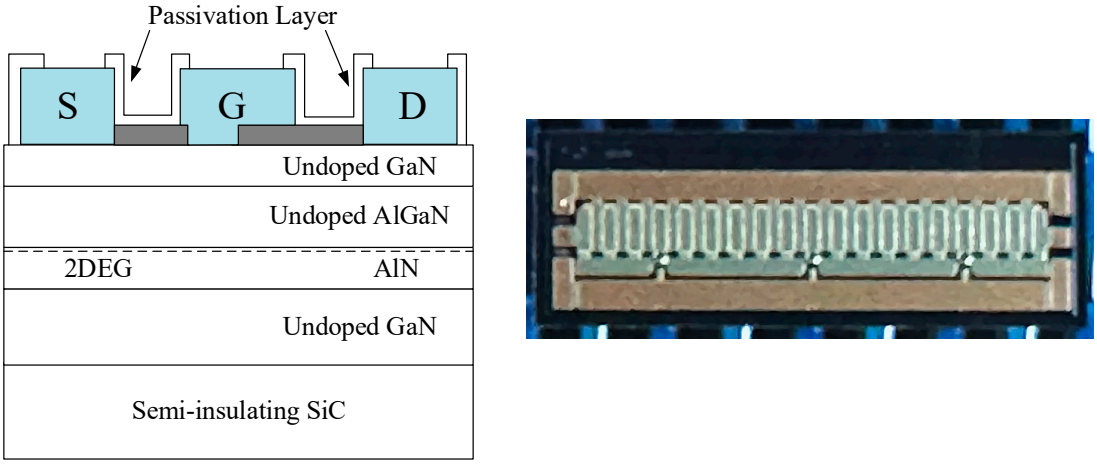


Figure 3. Schematic diagram of the longitudinal structure of GaN HEMT (**a**) and photograph of (**b**) its use in this design.

2.2. Parameter Extraction and Model Establishment

The EE_HEMT model was established based on a 1.2 mm gate-width model transistor with the same process technology as the GaN HEMT in this design. It has a single-finger gate width of 200 μm, with a total of 6 gate fingers, resulting in an overall gate width of 1.2 mm. Figure 4 shows a microscopic photograph of this model transistor.

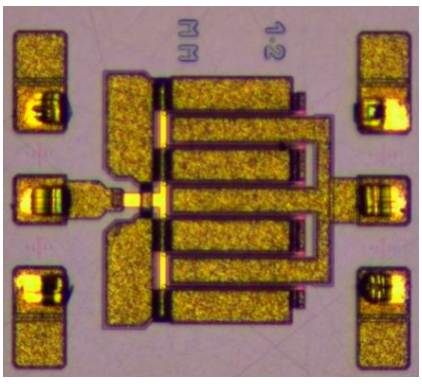


Figure 4. Microscopic photo of 1.2 mm gate-width model transistor.

DC scanning testing and S-parameter scanning testing in the frequency range of 0.4 GHz to 35 GHz with a pulse period of 1 ms and a duty cycle of 10% were conducted to extract intrinsic and parasitic parameters of the model transistor described above. By fitting the intrinsic and parasitic parameters, an equivalent circuit for the large-signal EE_HEMT model, as depicted in Figure 5a,b, was established. The extracted intrinsic parameters of

the transistor were R_G = 978 mΩ, R_D = 833 mΩ, R_S = 133 mΩ, and the parasitic parameters were L_G = 118 pH, L_D = 111 pH, L_S = 10.6 pH, C_{PG} = 31.5 fF, C_{PD} = 39.4 fF.

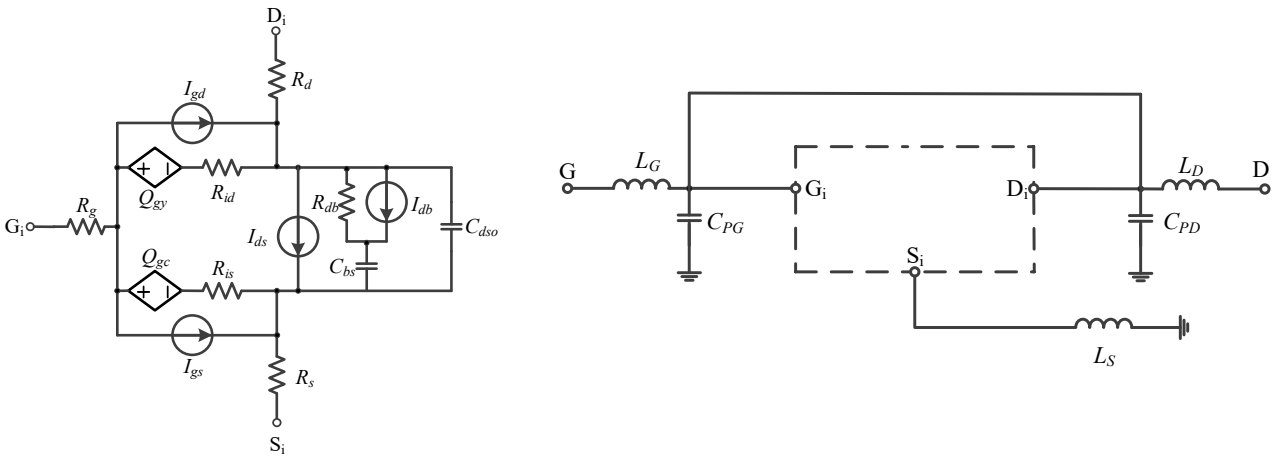


Figure 5. Intrinsic equivalent circuit diagram (**a**) and parasitic parameter equivalent circuit diagram (**b**) of the large-signal EE_HEMT model.

Additionally, load-pull testing was conducted on the model transistor to obtain information such as maximum saturated output power and the highest PAE, to validate the accuracy of the model under large-signal conditions. Figures 6 and 7 represent the DC characteristics and S-parameter test results compared with the model simulation results. In Figure 6a,b, the DC simulation and test results for drain current and gate current are presented, respectively. Figure 7b,c show the magnitude and phase errors of the S-parameters within the frequency range of 0.4–35 GHz. The magnitude error is less than ±0.05, while the phase error is distributed within the frequency range of −5 degrees to +8 degrees. Figure 8 displays the test results for load-pull output power and PAE, along with the simulation results. The results indicate a close agreement between simulation data and measured data, confirming the accuracy of the model structure and parameters.

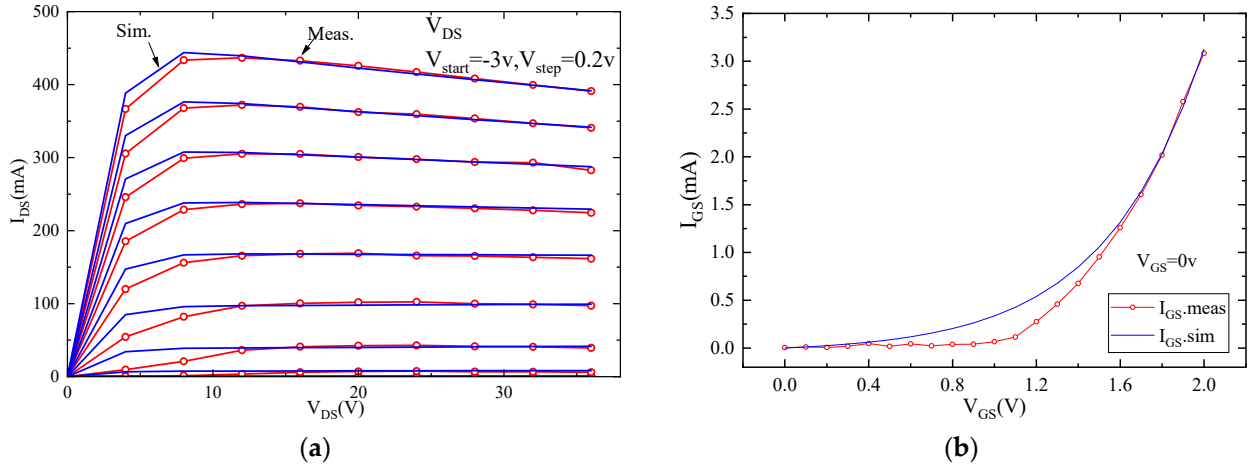


Figure 6. Comparison between simulation and measurement of DC characteristics of 1.2 mm gate-width model transistor, (**a**) drain current and (**b**) gain current.

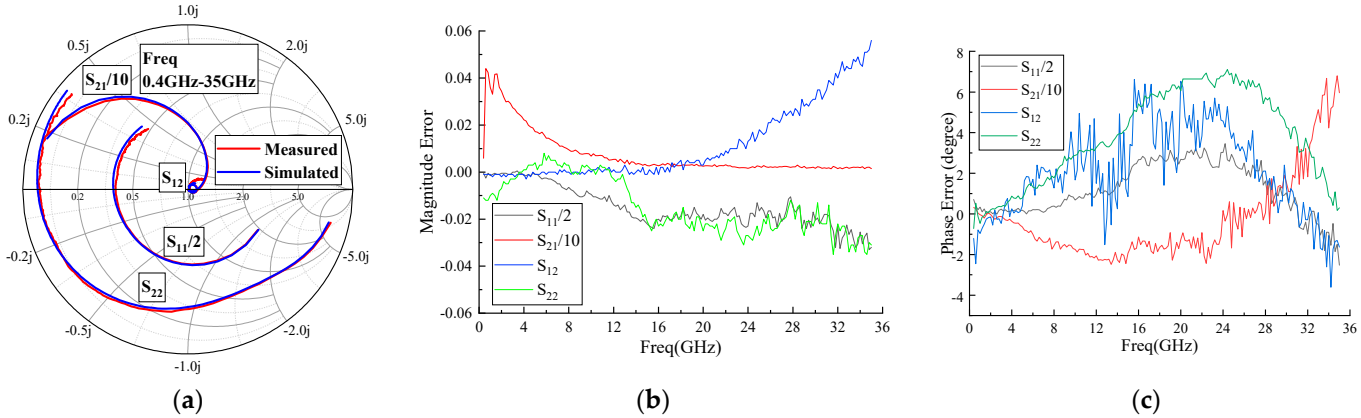


Figure 7. Comparison between simulation and measurement of 0.4–35 GHz S-parameters of 1.2 mm gate-width model transistor (**a**), magnitude error (**b**) and phase error (**c**).

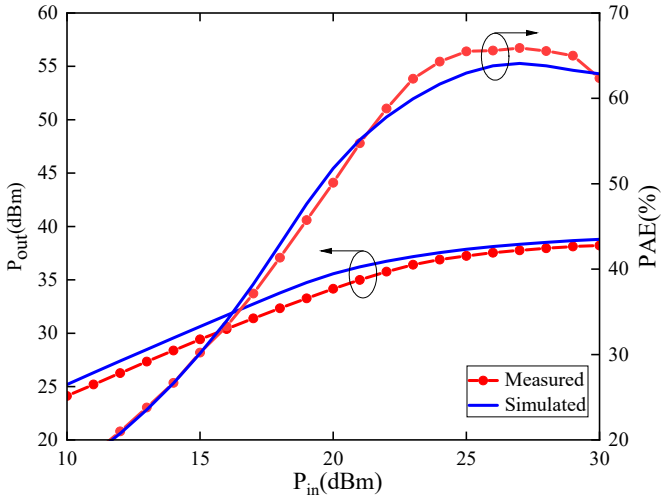


Figure 8. Comparison between simulation and measurement of output power and PAE of 1.2 mm gate-width model transistor.

2.3. Theory and Circuit

2.3.1. Load Modulation Behavior Analysis of Three-Stage Doherty PA

The Doherty PA structure used in this study is shown in Figure 2b; it is assumed that it is composed of symmetric devices and all cells saturate simultaneously at maximum input power. The relationship between the output and back-off power for the three-stage Doherty PA is derived as follows:

$$P_{out,max} = 3/2 \cdot V_{DC} \cdot I_{MAX} \quad (1)$$

$$P_{out,k2} = 1/2 \cdot V_{DC} \cdot I_{C,k2} \quad (2)$$

$$P_{out,k1} = 1/2 \cdot V_{DC} \cdot (I_{C,k1} + I_{P1,k1}) \quad (3)$$

where

$$I_{C,k1} = 2/3 \cdot k_1 \cdot P_{out,max}/V_{DC} \quad (4)$$

$$I_{P1,k1} = 2/3 \cdot (k_1 - k_2)/(1 - k_2) \cdot P_{out,max}/V_{DC} \quad (5)$$

$$I_{C,k2} = 2/3 \cdot k_2 \cdot P_{out,max}/V_{DC} \quad (6)$$

The back-off output power can be expressed in the following form:

$$P_{out,k1} = {k_1}^2 \cdot P_{out,max} \quad (7)$$

$$P_{out,k2} = {k_2}^2 \cdot P_{out,max} \tag{8}$$

Combining the equations above, we can determine the values of k_1 and k_2:

$$k_1 = 1/3, k_2 = 1/2 \text{ or } 1/3 \tag{9}$$

Under different biases, the three-stage Doherty PA can have two or three maximum efficiency points. Figure 9 shows the structure of the power-combining network, and according to the principles of dynamic load modulation, the characteristic impedances of the three microstrip lines can all be calculated.

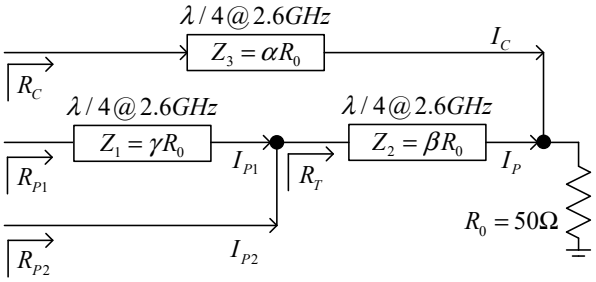


Figure 9. Schematic diagram of power-combining network.

The fundamental drain current ratio between the main amplifier and the peak amplifier can be defined as follows:

$$\delta_2 = I_{P2}(v_{in})/I_{P1}(v_{in}) \tag{10}$$

$$\delta_1 = (I_{P2}(v_{in}) + I_{P1}(v_{in}))/I_C(v_{in}) \tag{11}$$

Table 1 shows the variation in δ_1 and δ_2 as v_{in} increases.

Table 1. The values of δ_1 and δ_2 as v_{in} increases.

v_{in}/v_{max}	1/3	2/3	1
δ_1	0	1	2
δ_2	0	0	1

Assuming the load impedance R_0 is 50 Ω, and defining the characteristic impedances of each quarter-wavelength line as Z_3, Z_2, and Z_1 for each section as αR_0, βR_0, and γR_0, respectively, the load impedance for each amplifier can be derived as follows:

$$R_C = \alpha^2 \cdot R_0/(1 + \delta_1) \tag{12}$$

$$R_T = \beta^2 \cdot R_0 \cdot \delta_1/(1 + \delta_1) \tag{13}$$

$$R_{P1} = \gamma^2 \cdot R_0/\beta^2 \cdot (1 + \delta_1)/(\delta_1 \cdot (1 + \delta_2)) \tag{14}$$

$$R_{P1} = \beta^2 \cdot {R_0}^2 \cdot (\delta_1 \cdot (1 + \delta_2))/(\delta_2 \cdot (1 + \delta_1)) \tag{15}$$

Combining with Table 1, the load impedance for each amplifier can be derived as follows:

$$\begin{array}{ll} R_C = \alpha^2 \cdot R_0 & v_{in}/v_{max} = 1/3 \\ \quad = 1/2 \cdot \alpha^2 \cdot R_0 & v_{in}/v_{max} = 2/3 \\ \quad = 1/3 \cdot \alpha^2 \cdot R_0 & v_{in}/v_{max} = 1 \end{array} \tag{16}$$

$$\begin{array}{ll} R_{P1} = \infty & v_{in}/v_{max} = 1/3 \\ \quad = 3 \cdot \gamma^2 \cdot R_0/\beta^2 & v_{in}/v_{max} = 2/3 \\ \quad = 3/4 \cdot \gamma^2 \cdot R_0/\beta^2 & v_{in}/v_{max} = 1 \end{array} \tag{17}$$

$$\begin{array}{ll} R_{P2} = \infty & v_{in}/v_{max} = 1/3 \\ = \infty & v_{in}/v_{max} = 2/3 \\ = 4/3 \cdot \beta^2 \cdot R_0 & v_{in}/v_{max} = 1 \end{array} \quad (18)$$

If each amplifier is matched to 50 Ω when $v_{in}/v_{max} = 1$, then according to the above equations, Z_1, Z_2, and Z_3 can be calculated as follows:

$$Z_3 = \alpha \cdot R_0 = \text{Sqrt}(3) \cdot R_0 \quad (19)$$

$$Z_2 = \beta \cdot R_0 = \text{Sqrt}(3/4) \cdot R_0 \quad (20)$$

$$Z_1 = \gamma \cdot R_0 = 1 \cdot R_0 \quad (21)$$

2.3.2. Circuit Design

Load-pull simulation was performed on the transistor with a gate width of 7.2 mm, and the results indicate maximum output power of 46.2 dBm and peak PAE of 75.4%. Striking a balance between power and efficiency, the chosen saturation output impedance of the chip is 5.2 + j × 5.5 Ω. At this point, the output power is 46 dBm, and the PAE is 69.4%, meeting the design requirements.

The output matching employs an L-C-L matching structure implemented through microstrip lines, effectively controlling the circuit's second harmonic. The second harmonic impedance is maximized to make the amplifier operate in class-F^{-1} mode, thereby enhancing the efficiency of the single amplifier.

The contour of S_{11} in the intrinsic current source plane on the Smith chart is depicted in Figure 10a, and the contour of S_{11} for output matching network is depicted on the Smith chart in Figure 10b.

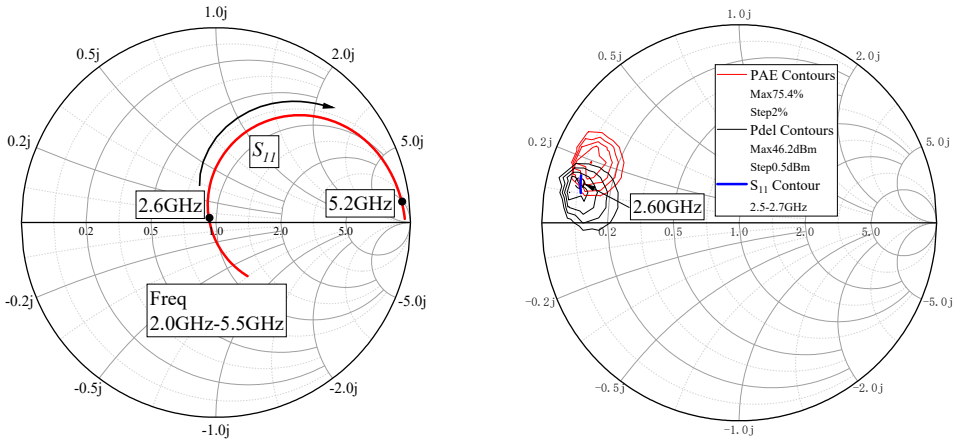


Figure 10. Contour of S_{11} in intrinsic current source plane (**a**) and contour of S_{11} for output-matching network (**b**).

Through source-pull simulation, input impedance of the transistor was determined to 0.3 − j × 2.2 Ω. The input matching network structure is similar to the output matching network structure, with a relatively simple design that can match input impedance to 50 Ω. Additionally, a parallel-connected capacitor-resistor stability circuit was added at the input of the transistor to ensure the stable operation of the amplifier. Figure 11 shows the schematic diagram of a single amplifier.

A frequency sweep large-signal simulation was performed on the designed single amplifier under bias conditions of V_{GS} = 28 V and V_{DS} = −2.1 V, with an input power of 34 dBm. The simulation results are presented in Figure 12. Figure 12a displays the large-signal simulation results of input and output return loss and Figure 12b displays the output power and PAE. The simulation results indicate that the saturated output power and PAE of the single amplifier were 45.9 dBm and 68.2%, respectively. These values closely

align with the load-pull data, confirming the accuracy of the circuit design. Furthermore, due to the introduction of a grounded circuit, the simulation of the stability factor (K) for the single amplifier within the operating frequency band was consistently greater than 1. This indicates that the amplifier can operate stably within the frequency range, ensuring its stability.

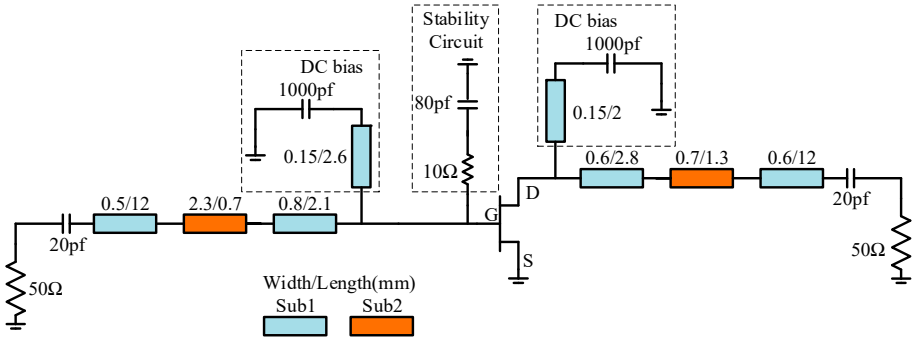


Figure 11. Schematic diagram of single amplifier.

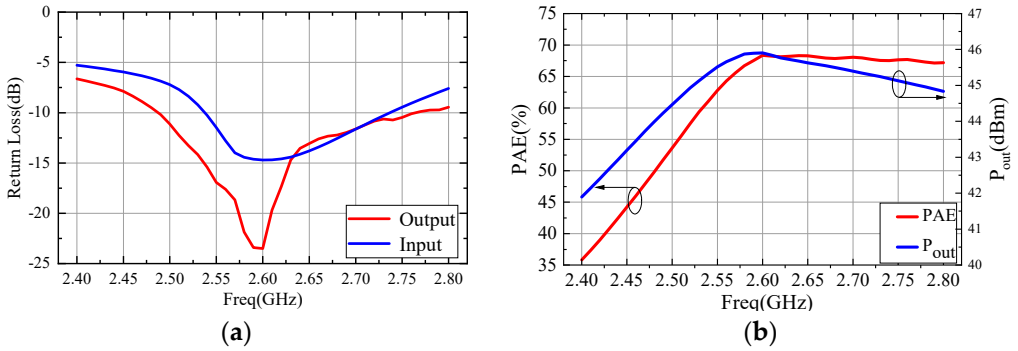


Figure 12. Simulation results of single amplifier (**a**) return loss and (**b**) output power and PAE.

In order to reduce the circuit size, the practical microstrip circuit was manufactured on an alumina ceramic substrate with a dielectric constant of 9.9 and thickness of 380 μm, as well as barium titanate ceramic substrates with dielectric constant of 85 and thickness of 180 μm. The microstrip circuit and the chip are sintered onto a molybdenum-copper alloy carrier, and they are interconnected through wire bonding. Additionally, 20 pF chip capacitors were added at the input and output positions of the amplifier to isolate the DC component. Furthermore, 1000 pF chip capacitors were also introduced to filter out high-frequency noise at the feeding point. The amplifier has dimensions of 19.2 mm × 10 mm and is securely fastened to the test fixture using screws.

The input power divider of the Doherty power amplifier adopts a three-way Wilkinson power divider structure with equal power splitting, and the impedance of each port of the power divider is 50 Ω. Additionally, to maintain the phase consistency of the three power amplifiers, 90° phase compensation lines with characteristic impedance of 50 Ω have been added before the main power amplifier and the second peak power amplifier. The power-combining circuit follows the structure described in Section 2.3.1. Both the power divider and the power-combining circuit have been implemented using microstrip circuits. These circuits were manufactured on PTFE material substrate with low dielectric constant of 2.2 and thickness of 762 μm to ensure that the microstrip widths are sufficiently large to meet the requirements for high power. They are both sintered onto the test fixture and connected to single amplifiers, as described above, using wire bonding. SMA connectors were added at the input and output positions of the power amplifier for test purposes. Properly located pads for feeding and grounding were introduced, and the grounding pads were connected to the test fixture through vias. In addition, capacitors of 100 pF, 1000 pF, and 43 μF were placed between the feeding and grounding pads to filter out high-frequency

noise. Figure 13 shows a photograph of the whole Doherty power amplifier. The overall dimensions of the circuit are 66 mm × 60 mm, and its weight is 103.4 g.

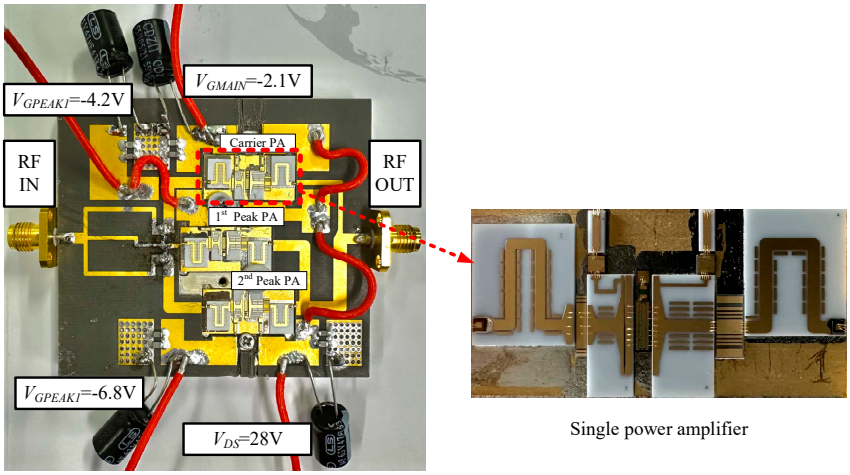


Figure 13. Photograph of whole Doherty PA and single PA.

3. Results

3.1. CW Test

As described above, this study employed the Doherty amplifier structure shown in Figure 2b. In this configuration, for each single amplifier, the other two amplifiers act as feedback loops introduced at the input. The introduction of feedback has a significant impact on the Doherty amplifier when a single amplifier experiences self-oscillation, leading to a substantial increase in noise and severe interference with the integrity of the signal. To avoid such occurrences, it is crucial to ensure the stability of the Doherty amplifier.

In Section 2.3.2, the stability of the single amplifier was verified through simulation, and prior to the continuous wave testing of the Doherty amplifier, its stability was experimentally confirmed. Under bias conditions of V_{DS} = 28 V, V_{GMAIN} = −2.1 V, V_{GPEAK1} = −4.2 V, and V_{GPEAK2} = −6.8 V, with no RF signal input, the drain current was zero. As the gate voltage of the main amplifier gradually increased, the drain current also steadily and linearly increased. This observation indicates that the Doherty amplifier does not undergo self-oscillation and can operate stably.

After verifying the stability of the Doherty amplifier under the same bias conditions, continuous-mode power scanning test and frequency scanning test were conducted on the designed Doherty power amplifier. Figure 14a–c depict the results of the power scanning tests; Figure 14a,b show the test results and simulation results for PAE and drain efficiency, while Figure 14c illustrates the gain characteristics of the Doherty power amplifier.

As shown in Figure 14, at 2.6 GHz, the saturated output power was 49.7 dBm, with a drain efficiency exceeding 67% and gain exceeding 9 dB. At the output power of 40.5 dBm, corresponding to a 9 dB power back-off, the drain efficiency remained above 55%, and the gain was above 8 dB. Comparison with simulation results reveals that, under large-signal excitation, the measured drain efficiency and gain exhibit errors of less than 5% and less than 1 dB, respectively. The overall trend is consistent with the simulation results, confirming the accuracy of the model. The sources of error may originate from two aspects: bonding wires and thermal effects. It is challenging to accurately describe the shape of bonding wires, gold ribbons, and the location of pads during the simulation process. Additionally, the heat generated by the Doherty amplifier can reduce the drain efficiency, and the EE_HEMT model has certain limitations in accurately characterizing the self-heating effects of the transistor. This limitation results in an inability to accurately simulate the thermal effects of the transistor.

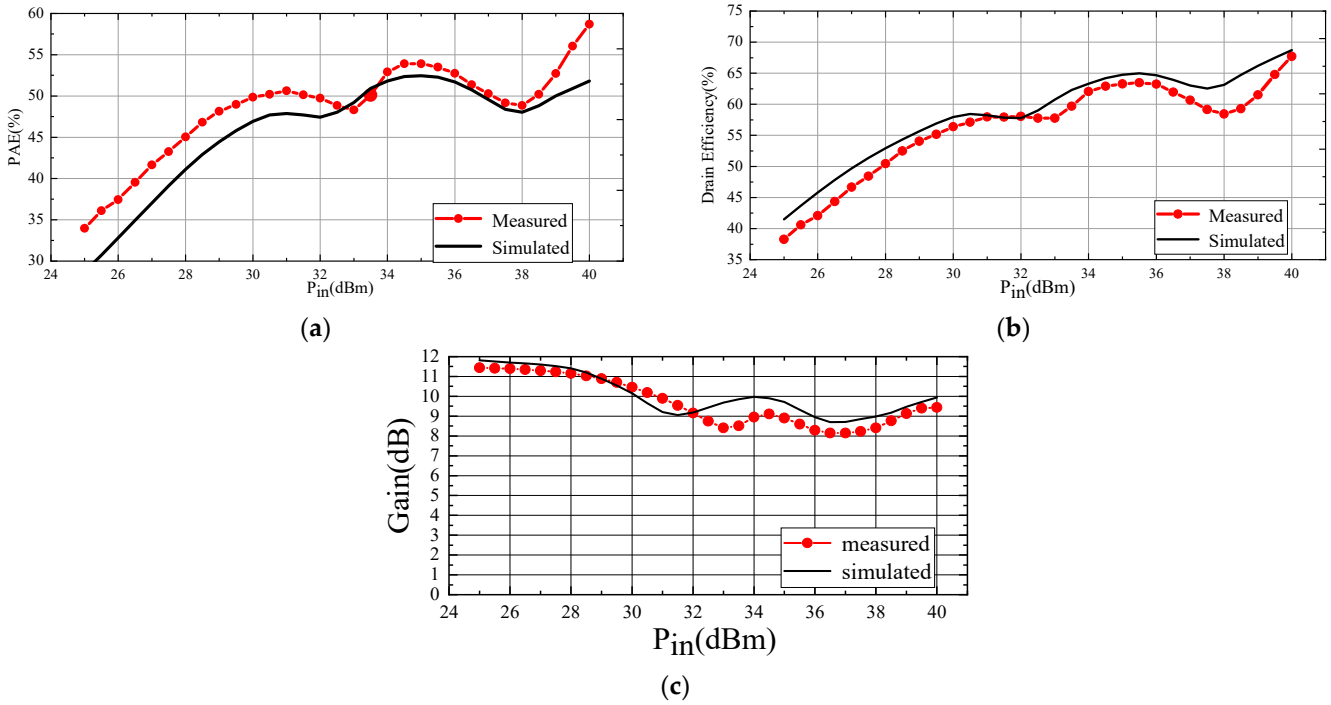


Figure 14. CW test results and simulation results of PAE (**a**), drain efficiency (**b**), and gain (**c**).

We observed that the trends of the curves obtained from simulation and experimentation were similar but not entirely identical. In comparison to the test results, the simulation results show an earlier occurrence of the first maximum efficiency point. This discrepancy arises because the model was established based on parameters extracted in the transistor's on state, introducing errors in describing the transistor's deep Class-C-mode operating state. In model-based simulations, the auxiliary amplifier is entirely shut off during Class-C operation, whereas in reality, a small portion of the main amplifier's power leaks into the auxiliary amplifiers, preventing a complete off state and causing the maximum efficiency point to appear later.

Additionally, according to Figure 14a,b, it is noted that the simulated results for power-added efficiency are slightly lower than the test results, while the relationship of drain efficiency between simulation and test is reversed. The probable cause of this trend is that the actual input signal was smaller than the ideal input signal in the test. The actual input signal, generated by the signal generator and amplified by the solid-state amplifier, was slightly reduced due to the connection losses between devices and the noise from the signal generator to the solid-state amplifier. In contrast, the simulation uses an ideal input signal.

Figure 15 indicates the relationships between the input power and efficiency of the Doherty power amplifier within a frequency range of 2.55 GHz to 2.62 GHz. As shown in the graph, this Doherty power amplifier exhibits stable performance within bandwidth of 70 MHz.

Table 2 presents a comparison between this work and other three-stage Doherty power amplifiers. Compared with other results, this study demonstrates larger saturated output power, higher drain efficiency, and higher linearity.

Table 2. Compared with other three-stage Doherty PAs.

Units	Architecture	f_0 (GHz)	BW (MHz)	P_{MAX} (dBm)	DE (%) @PBO	Back-Off Range	ACLR
[6]	2-way	2.43	750	44.6	49	9	−46.2 dBc
[7]	2-way	2.14	10	36.9	55.7	6.5	−25.0 dBc

Table 2. *Cont.*

Units	Architecture	f_0 (GHz)	BW (MHz)	P_{MAX} (dBm)	DE (%) @PBO	Back-Off Range	ACLR
[16]	3-stage	2.655	15	50.5	55.4	8.5	−40 dBc
[18]	3-stage	0.75	300	46.1	50	12	−50.2 dBc
[19]	3-stage	2.14	100	45.3	55	10	−49.8 dBc
[20]	3-way	2.1	600	46	53	9.5	−30 dBc
This work	3-stage	2.6	70	49.7	57.9	9	−50.93 dBc

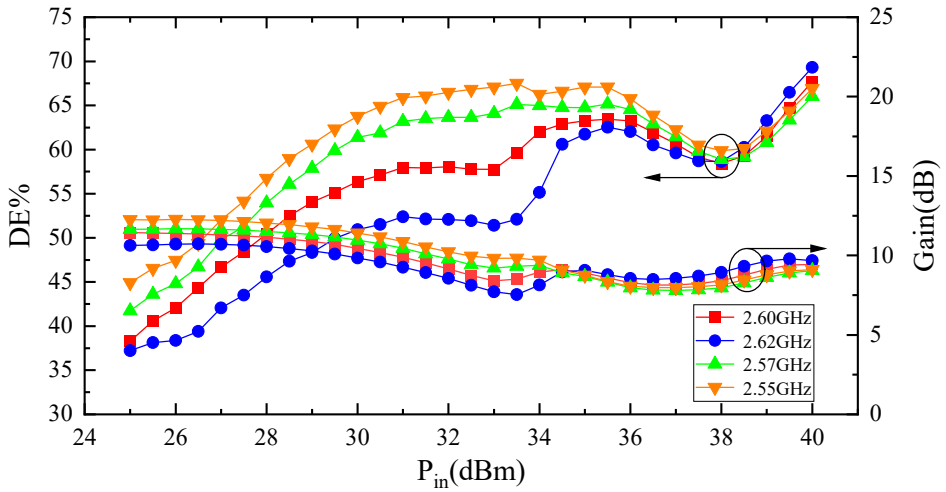


Figure 15. Test results results of drain efficiency and gain at 2.55 GHz–2.62 GHz.

3.2. Modulated Signal Test

Linearity testing was conducted using a modulation signal test system. A Rohde & Schwarz vector signal generator, model SMW200A, was employed to generate the modulation signal, and a spectrum analyzer, model FSW, was used to test the EVM (error vector magnitude) and ACLR (adjacent-channel leakage ratio).

The vector signal generator generated a 10 MHz bandwidth QPSK signal with PAPR of approximately 8.3 dB. The amplifier was biased in the same way as in the continuous wave test, with V_{DS} = 28 V, V_{GMAIN} = −2.1 V, V_{GPEAK1} = −4.2 V, and V_{GPEAK2} = −6.8 V. The test process incorporated DPD technology, and the ACLR test results are depicted in Figure 16. The ACLRs of lower and upper adjacent channels were −22.19 dBc and −23.66 dBc without DPD, and while using DPD, the ACLRs of lower and upper adjacent channels were 50.93 dBc and 52.0 dBc, indicating the high linearity of the Doherty power amplifier.

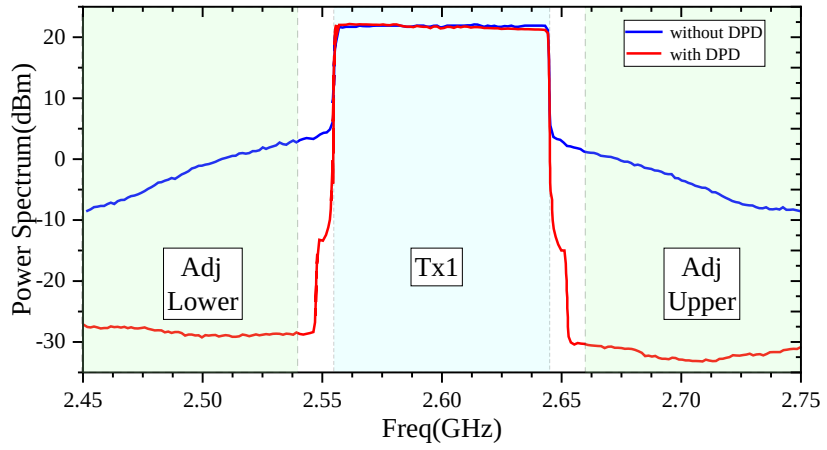
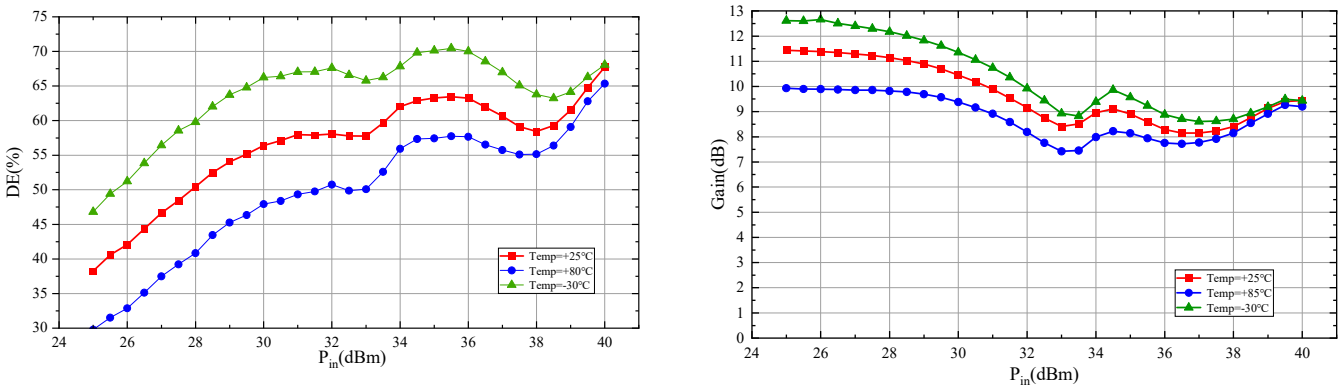


Figure 16. Test results of ACLR with 10 MHz QPSK signal.

3.3. Temperature Test and Aging Test

Temperature can significantly impact the DC and microwave characteristics of GaN HEMT devices, with performance degradation being more pronounced at high temperatures. The reasons for this are as follows. Firstly, an increase in junction temperature leads to a reduction in the carrier mobility and saturation drift velocity, diminishing the device's switching speed and subsequently affecting its high-frequency performance. Additionally, in HEMT devices, the gate contact to the semiconductor substrate junction is an Ohmic contact, while the source and drain contacts to the semiconductor substrate are Schottky contacts. Elevated temperatures accelerate diffusion between the metal and semiconductor, degrading both ohmic and Schottky contacts. This results in a reduction in the barrier height, lowering the breakdown voltage and power-handling capacity of the device, which is detrimental to stable device operation. Furthermore, prolonged operation at high temperatures may also impact circuit components. Excessive temperatures can lead to wire bond failures, and the Q-value of chip capacitors may decrease, affecting the overall circuit performance. In summary, under high-temperature conditions, the reliability and electrical performance of GaN HEMT devices and circuits tend to degrade, while the opposite is true under low-temperature conditions.

In order to validate the circuit's reliability, high-temperature (+85 °C) and low-temperature (−30 °C) tests were conducted on the Doherty power amplifier under the same conditions as the continuous wave test. Figure 17a,b present the drain efficiency and gain results of power scanning tests at high, room, and low temperatures.



(**a**) (**b**)

Figure 17. Test results of drain efficiency (**a**) and gain (**b**) at different temperatures.

As depicted in the figures, the designed Doherty power amplifier operates normally at both +85 °C and −30 °C temperatures. In the power back-off range, its drain efficiency changes by less than ±8%, and gain changes are within ±1.5 dB, showing consistent trends. These results indicate that the Doherty power amplifier exhibits high reliability under different temperature conditions.

In addition, in order to test long-term stable operation capability, aging tests were conducted on the Doherty power amplifier under room-temperature conditions. Under the same bias conditions, the power amplifier worked continuously for 160 h at input power levels of 31 dBm and 40 dBm, corresponding to the back-off and saturated points of the Doherty power amplifier, respectively. The results showed that amplifier could still operate normally after the aging test with almost consistent performance. The designed Doherty power amplifier demonstrates capacity for long-term stable operation, exhibiting a certain degree of reliability.

4. Discussion

This study conducted a theoretical analysis of a three-stage Doherty power amplifier power-synthesis network and designed a three-stage high-power Doherty power amplifier

based on the theoretical analysis. The test results indicate that the designed Doherty power amplifier can effectively extend the power back-off range of traditional Doherty amplifier architectures, consistent with the theoretical analysis. Additionally, as described in Section 2.3.2, the harmonic matching technique employed in the single amplifier enhances the overall efficiency of the Doherty power amplifier to a certain extent. In comparison to recently reported Doherty power amplifiers, this study demonstrates advantages in performance metrics such as output power and efficiency.

Future research will focus on expanding the operational bandwidth of the Doherty power amplifier while ensuring output power. Bandwidth expansion may be achieved by reducing the use of quarter-wavelength lines to improve the power-combining network and implementing a wideband matching strategy for the single amplifier. These improvements are expected to further enhance the performance of the Doherty power amplifier across different frequency ranges, better meeting the demands of practical applications.

5. Conclusions

In summary, we have presented a miniaturized GaN HEMT high-power Doherty power amplifier based on the 0.25 μm process platform of the Nanjing Electronic Devices Institute. We established the EE_HEMT model of the chip through parameter extraction and load-pull testing. Using this model as a foundation, we designed a Doherty power amplifier. Experimental results indicate that at 2.6 GHz under continuous wave test conditions, the saturated output power exceeds 49.7 dBm, drain efficiency surpasses 67%, and gain is over 9 dB. At a 9 dB power back-off point, the drain efficiency remains above 55%. The performance is consistent within the frequency range of 2.55 GHz to 2.62 GHz. Furthermore, the test results align closely with the simulation results based on the model. Under large-signal excitation, the measured drain efficiency error is less than 5%, and the gain error is less than 1 dB, validating the accuracy of the model and circuit design. Additionally, this amplifier features compactness and lightness and exhibits stability at both high and low temperatures. The amplifier holds practical significance for modern wireless communication hardware platforms.

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References

1. Mohammady, S.; Farrell, R.; Malone, D.; Dooley, J. Performance Investigation of Peak Shrinking and Interpolating the PAPR Reduction Technique for LTE-Advance and 5G Signals. *Information* **2020**, *11*, 20. [CrossRef]
2. Bangerter, B.; Talwar, S.; Arefi, R.; Stewart, K. Networks and devices for the 5G era(Article). *IEEE Commun. Mag.* **2014**, *52*, 90–96. [CrossRef]
3. Doherty, W.H. A New High Efficiency Power Amplifier for Modulated Waves. *Proc. IRE* **1936**, *24*, 1163–1182. [CrossRef]
4. Giofrè, R.; Piazzon, L.; Colantonio, P.; Giannini, F. An ultra-broadband GaN Doherty amplifier with 83% of fractional bandwidth. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 775–777. [CrossRef]
5. Giofrè, R.; Piazzon, L.; Colantonio, P.; Giannini, F. A closed-form design technique for ultra-wideband Doherty power amplifiers. *IEEE Trans. Microw. Theory Tech.* **2014**, *62*, 3414–3424. [CrossRef]
6. Zhang, J.R.; Zheng, S.Y.; Yang, N. An Efficient Broadband Symmetrical Doherty Power Amplifier With Extended Back-Off Range. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 1316–1320. [CrossRef]
7. Oh, H.; Kang, H.; Lee, H.; Koo, H.; Kim, M.; Lee, W.; Lim, W.; Park, C.-S.; Hwang, K.C.; Lee, K.-Y.; et al. Doherty Power Amplifier Based on the Fundamental Current Ratio for Asymmetric cells. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 4190–4197. [CrossRef]
8. Pitt, A.; Jindal, G.; Morris, K.; Cappello, T. A Broadband Asymmetrical Doherty Power Amplifier With Optimized Continuous Mode Harmonic Impedances. *IEEE J. Microw.* **2023**, *3*, 1120–1133. [CrossRef]

9. Zhang, Z.; Fusco, V.; Cheng, Z.; Gu, C.; Buchanan, N.; Ying, J. A Broadband Doherty-like Power Amplifier With Large Power Back-Off Range. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 2722–2726. [CrossRef]
10. Zhou, L.H.; Zhou, X.Y.; Chan, W.S. A Compact and Broadband Doherty Power Amplifier Without Post-Matching Network. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 919–923. [CrossRef]
11. Bai, G.; Dai, Z.; Wang, J.; Bi, C.; Shi, W.; Pang, J.; Li, M. Design of Broadband Doherty Power Amplifier Based on Single Loop Load Modulation Network. *IEEE J. Emerg. Sel. Top. Circuits Syst.* **2024**. [CrossRef]
12. Moreno Rubio, J.J.; Angarita Malaver, E.F.; Lara González, L.Á. Wideband Doherty Power Amplifier: A Design Approach. *Micromachines* **2022**, *13*, 497. [CrossRef]
13. Xie, L.; Zhong, S.; Liang, C. High-efficiency broadband Doherty amplifier based on internal matching. *Microw. Opt. Technol. Lett.* **2023**, *66*, e33877. [CrossRef]
14. Liang, C.; Roblin, P.; Hahn, Y. Accelerated Design Methodology for Dual-Input Doherty Power Amplifiers. *IEEE Trans. Microw. Theory Tech.* **2019**, *67*, 3983–3995. [CrossRef]
15. Wu, D.Y.-T.; Boumaiza, S. A Modified Doherty Configuration for Broadband Amplification Using Symmetrical Devices. *IEEE Trans. Microw. Theory Tech.* **2012**, *60*, 3201–3213. [CrossRef]
16. Kim, I.; Moon, J.; Jee, S.; Kim, B. Optimized Design of a Highly Efficient Three-Stage Doherty PA Using Gate Adaptation. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 2562–2574. [CrossRef]
17. Barthwal, A.; Rawat, K.; Koul, S. Bandwidth Enhancement of Three-Stage Doherty Power Amplifier Using Symmetric Devices. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 2399–2410. [CrossRef]
18. Naderi, P.; Fallahi, F. A Design Strategy for Bandwidth Enhancement in Three-Stage Doherty Power Amplifier with Extended Dynamic Range. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 1024–1033.
19. Zhou, H.; Perez-Cisneros, J.R.; Hesami, S.; Buisman, K.; Fager, C. A Generic Theory for Design of Efficient Three-Stage Doherty Power Amplifiers. *IEEE Trans. Microw. Theory Tech.* **2022**, *70*, 1242–1253. [CrossRef]
20. Xia, J.; Chen, W.; Meng, F.; Yu, C.; Zhu, X. Improved Three-Stage Doherty Amplifier Design With Impedance Compensation in Load Combiner for Broadband Applications. *IEEE Trans. Microw. Theory Tech.* **2019**, *67*, 778–786. [CrossRef]
21. Meghdadi, M.; Medi, A. Design of 6–18-GHz High-Power Amplifier in GaAs pHEMT Technology. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 2353–2360. [CrossRef]
22. Chen, Y.; Liu, W.; Wang, C.; Kong, X.; Zhao, Z. A scalable non-linear compact model applied to HEMT devices. *J. Terahertz Sci. Electron. Inf. Technol.* **2019**, *17*, 162–168.
23. Huang, D.; Zhong, S.C.; Xu, Z.Y.; Cheng, A.Q.; Wang, S. Research on Nonlinear Behavior Model of GaN HEMT Based on EPHD. *Radio Eng.* **2022**, *52*, 1490–1495.
24. Kharabi, F.; Poulton, M.J.; Halchin, D.; Green, D. A Classic Nonlinear FET model for GaN HEMT Devices. In Proceedings of the 2007 IEEE Compound Semiconductor Integrated Circuits Symposium, Portland, OR, USA, 14–17 October 2007.
25. Zomorrodian, V.; Pei, Y.; Mishra, U.K.; York, R.A. A scalable EE_HEMT based large signal model for multi-finger AlGaN/GaN HEMTs for linear and non-linear circuit design. *Phys. Status Solidi C* **2010**, *7*, 2450–2454. [CrossRef]
26. He, J.; Zhong, S.C.; Zhu, J.; Zhang, H.C. Design of an L-band high-elicieney small-size power amplifier carrier. *Space Electron. Technol.* **2023**, *20*, 24–28.
27. Shao, G.; Zhao, Y.; Wang, J.; Zhou, S.; Chen, T.; Jing, S.; Zhong, S. Study on 60Co-γ Irradiation Effect of GaN HEMT Devices. *Res. Prog. SSE* **2023**, *43*, 277–280, 286.